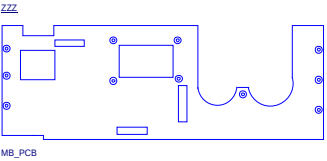


MODEL NAME : CAZ60

PCB NO : LA-E671P

BOM P/N : 43xxxxx



Dell/Compal Confidential

Schematic Document

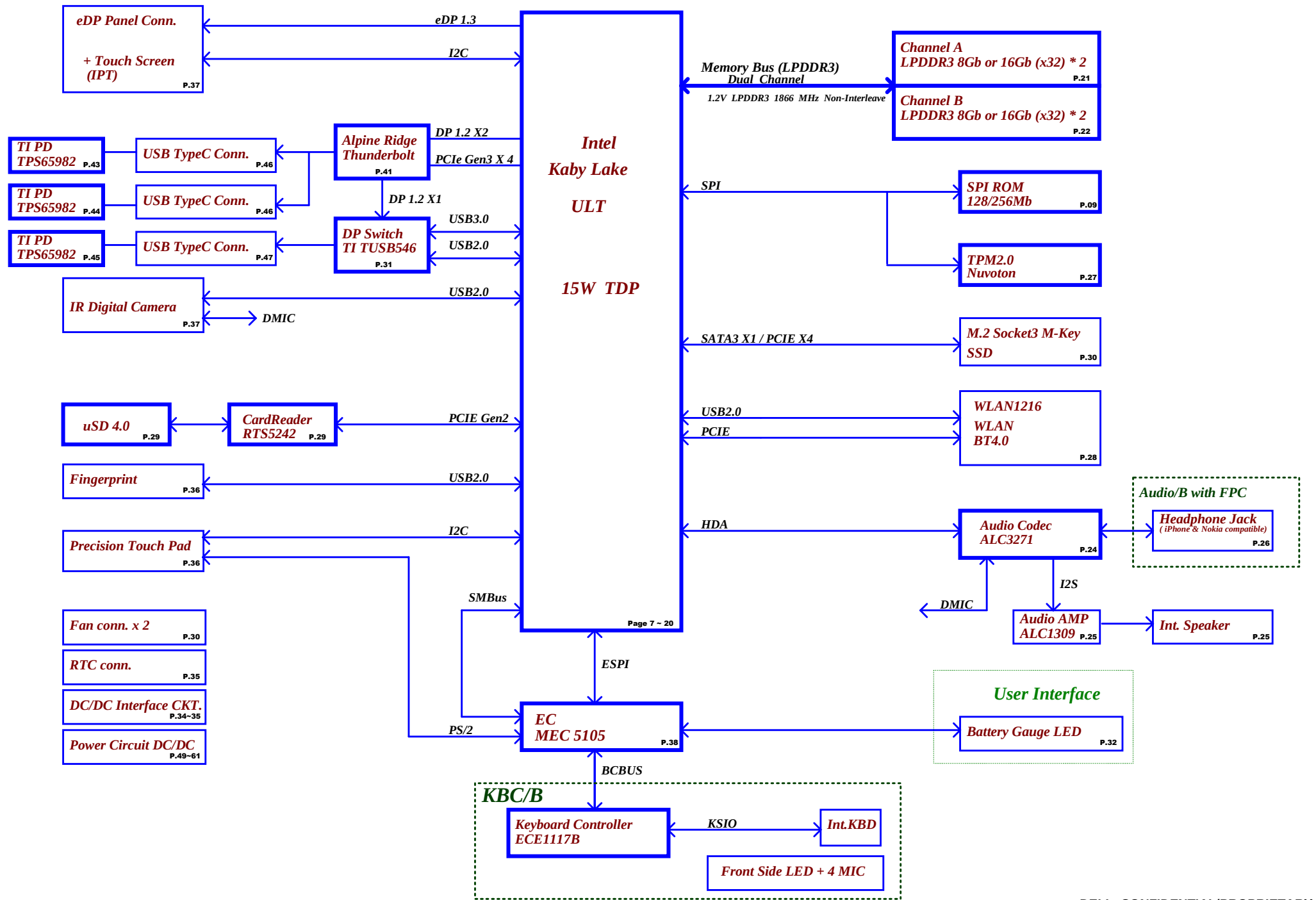
Italia

- @ : Nopop Component
- @ CONN@ : Reserve Connector Component
- @ EMC@ : Reserve EMC Component
- CONN@ : Connector Component
- XPS@ : for Italia
- L@ : for Italia-L
- RF@ : RF Solution Component
- XDP@ : XDP Debug Component
- EMC@ : EMC Component
- U22@ : U22 CPU Support
- U23@ : U23 CPU Support
- U42@ : U42 CPU Support
- U22U23@ : U22 and U23 CPU Support
- DEBUG@ : for Other Debug
- 650@ : TPM
- 750@ : TPM
- DCI@ : for DCI Debug

2017-09-15

Rev: 1.0 (A00)

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2+2 CPU Option

UCPU1 QNB1_2+2@
SA0000A1YL

UCPU1 QLV1_2+2_R3@
SA0000A37L

2+3 CPU Option

UCPU1 QMB1_2+3_R3@
SA0000AHS1L

4+2 CPU Option

UCPU1 QNEE_4+2_R3@
SA0000AHS2L

UCPU1 QNEF_4+2_R3@
SA0000AHS3L

UCPU1 QNBF_4+2_R3@
SA0000AHC2L

UCPU1 QNBE_4+2_R3@
SA0000AHS2L

AR Option

UT2 AR_SLL42@
SA0000BSY1L
DSL6340 SLL42 B2

TPM Option

U7 TPM750@
SA0000A200
TPM750 - ES FW:7.1.0.0

DRAM Option

Micron 4G/1866
SA0000S9L1L

UD41 M4G_1866@
SA0000S9U1L

UD42 M4G_1866@
SA0000S9U1L

UD43 M4G_1866@
SA0000S9U1L

UD44 M4G_1866@
SA0000S9U1L

Micron 8G/1866
SA0000S9U71L

UD41 M8G_1866@
SA0000S9U71L

UD42 M8G_1866@
SA0000S9U71L

UD43 M8G_1866@
SA0000S9U71L

UD44 M8G_1866@
SA0000S9U71L

Micron 16G/1866
SA0000S9Z1L

UD41 M16G_1866@
SA0000S9Z1L

UD42 M16G_1866@
SA0000S9Z1L

UD43 M16G_1866@
SA0000S9Z1L

UD44 M16G_1866@
SA0000S9Z1L

Hynix 4G/1866
SA0000SG44L

UD41 H4G_1866@
SA0000SG44L
H9CCNNNBGTALAR-NUD

UD42 H4G_1866@
SA0000SG44L
H9CCNNNBGTALAR-NUD

UD43 H4G_1866@
SA0000SG44L
H9CCNNNBGTALAR-NUD

UD44 H4G_1866@
SA0000SG44L
H9CCNNNBGTALAR-NUD

Hynix 8G/1866
SA0000SF24L

UD41 H8G_1866@
SA0000SF24L
H9CCNNNBGTALAR-NUD

UD42 H8G_1866@
SA0000SF24L
H9CCNNNBGTALAR-NUD

UD43 H8G_1866@
SA0000SF24L
H9CCNNNBGTALAR-NUD

UD44 H8G_1866@
SA0000SF24L
H9CCNNNBGTALAR-NUD

Hynix 16G/1866
SA0000AEHL

UD41 H16G_1866@
SA0000AEHL
H9CCNNNBGTALAR-NUD

UD42 H16G_1866@
SA0000AEHL
H9CCNNNBGTALAR-NUD

UD43 H16G_1866@
SA0000AEHL
H9CCNNNBGTALAR-NUD

UD44 H16G_1866@
SA0000AEHL
H9CCNNNBGTALAR-NUD

DRAM Config Option

MEM_CONFIG0
RH41 M4G_1866@
SD028100280
10K_0402_5%

MEM_CONFIG1
RH44 M4G_1866@
SD028100280
10K_0402_5%

MEM_CONFIG2
RH46 M4G_1866@
SD028100280
10K_0402_5%

MEM_CONFIG3
RH47 M4G_1866@
SD028100280
10K_0402_5%

MEM_CONFIG4
RH40 M4G_1866@
SD028100280
10K_0402_5%

RH42 M8G_1866@
SD028100280
10K_0402_5%

RH43 M8G_1866@
SD028100280
10K_0402_5%

RH45 M8G_1866@
SD028100280
10K_0402_5%

RH47 M8G_1866@
SD028100280
10K_0402_5%

RH40 M8G_1866@
SD028100280
10K_0402_5%

RH41 M16G_1866@
SD028100280
10K_0402_5%-D

RH43 M16G_1866@
SD028100280
10K_0402_5%-D

RH45 M16G_1866@
SD028100280
10K_0402_5%-D

RH47 M16G_1866@
SD028100280
10K_0402_5%-D

RH40 M16G_1866@
SD028100280
10K_0402_5%-D

RH42 H4G_1866@
SD028100280
10K_0402_5%-D

RH44 H4G_1866@
SD028100280
10K_0402_5%-D

RH45 H4G_1866@
SD028100280
10K_0402_5%-D

RH47 H4G_1866@
SD028100280
10K_0402_5%-D

RH40 H4G_1866@
SD028100280
10K_0402_5%-D

RH42 H8G_1866@
SD028100280
10K_0402_5%-D

RH44 H8G_1866@
SD028100280
10K_0402_5%-D

RH45 H8G_1866@
SD028100280
10K_0402_5%-D

RH47 H8G_1866@
SD028100280
10K_0402_5%-D

RH40 H8G_1866@
SD028100280
10K_0402_5%-D

RH42 H16G_1866@
SD028100280
10K_0402_5%-D

RH43 H16G_1866@
SD028100280
10K_0402_5%-D

RH45 H16G_1866@
SD028100280
10K_0402_5%-D

RH47 H16G_1866@
SD028100280
10K_0402_5%-D

RH40 H16G_1866@
SD028100280
10K_0402_5%-D

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Title
P03-BoM Option
Size
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LA-E671P
Date
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Board ID Table for AD channel

RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

CPU	4+2	2+3	3+2
Italia CAZ60			

BOARD ID rise time measured from 5%~68%.

SMBUS Control Table


	SOURCE	BATTERY Charger	PD1	PD2	PWR_MON	5105	XDP	Audio AMP	eDP	Touch Pad	Touch S	IR_THER_S
SMB00_CLK SMB00_DATA	MEC5105			V								
SMB01_CLK SMB01_DATA	MEC5105											V
SMB02_CLK SMB02_DATA	MEC5105									V		
SMB04_CLK SMB04_DATA	MEC5105		V									
SMB05_CLK SMB05_DATA	MEC5105							V				
SMB07_CLK SMB07_DATA	MEC5105				V							
SMB10_CLK SMB10_DATA	MEC5105	V										
PCH_SML1CLK PCH_SML1DATA	PCH					V						
SMBCLK SMBDATA	PCH						V					
I2C0_CLK I2C0_DATA	PCH										V	
I2C1_CLK I2C1_DATA	PCH									V		
I2C2_CLK I2C2_DATA	PCH								V			


CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Card Reader
	CLKOUT_PCIE1	NGFF WLAN	Lane 2	NC
	CLKOUT_PCIE2	NC	Lane 3	NGFF WLAN
	CLKOUT_PCIE3	M.2 SSD	Lane 4	NC
	CLKOUT_PCIE4	NC	Lane 5	Alpine Ridge
	CLKOUT_PCIE5	Card Reader	Lane 6	Alpine Ridge
	FLEX CLK#	DESTINATION	Lane 7	Alpine Ridge
	CLKOUT_LPC_0	ESPI 5105	Lane 8	Alpine Ridge
	CLKOUT_LPC_1	NC	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

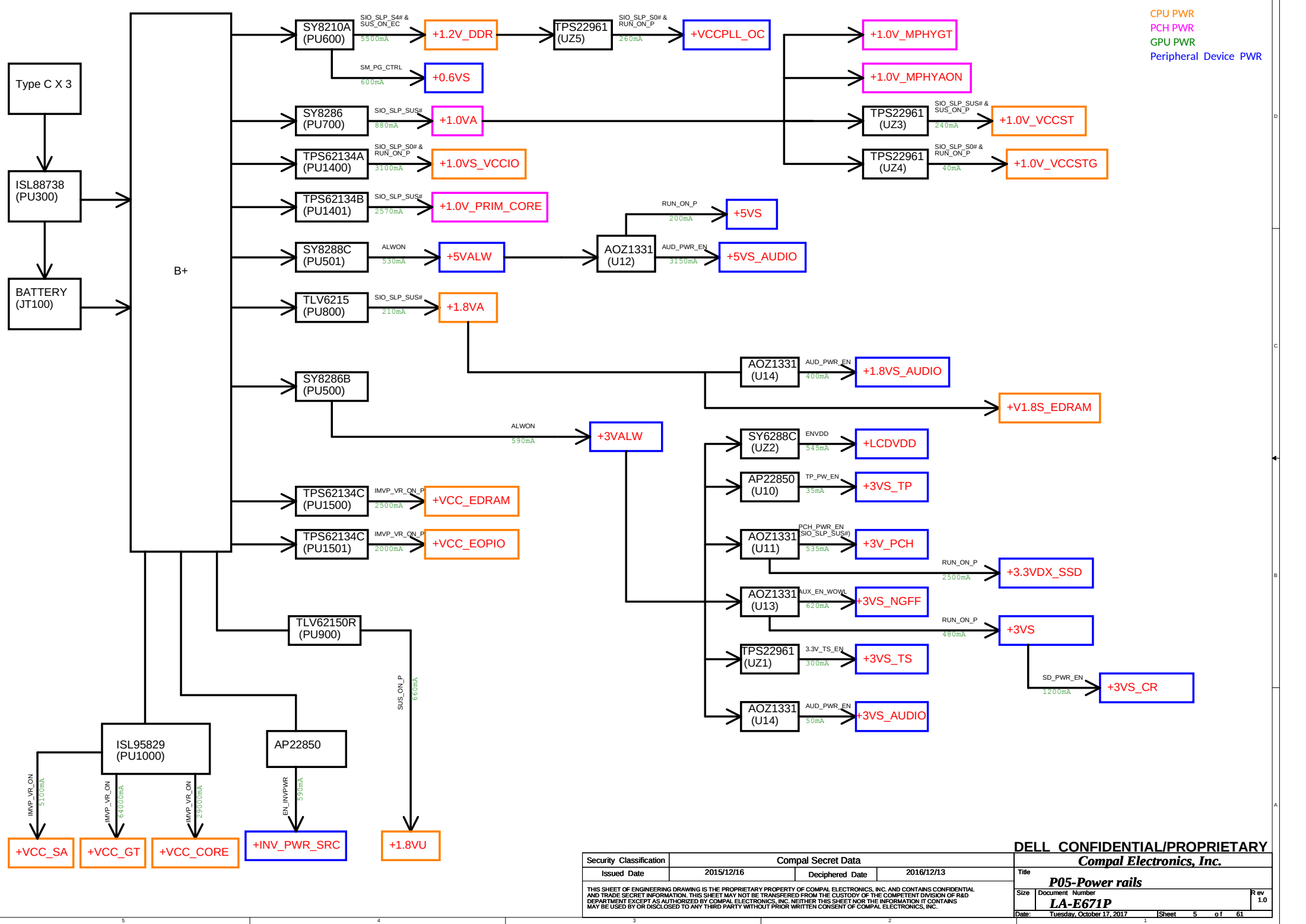
SATA PORT#	DESTINATION
SATA-0	NC
SATA-1A	NC
SATA-1B	NC
SATA-2	M.2 SSD

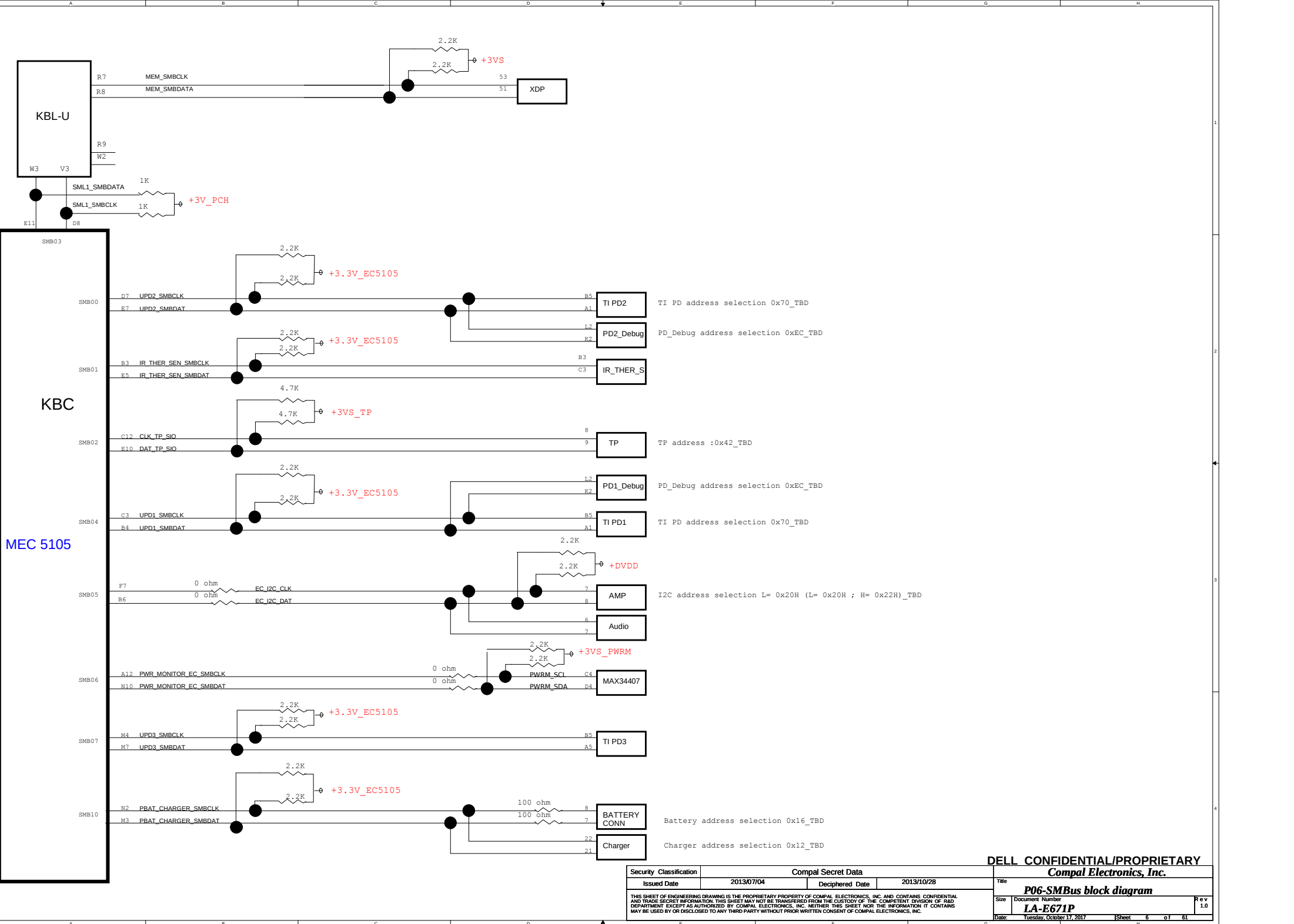
PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	PD PORT3
	2	NC
	3	NC
	4	NC
	5	IR Camera & Cam
	6	NC
	7	NGFF WLAN BT
	8	NC
	9	NC
	10	Fingerprint
PCH USB 3.0 Port Mapping	1	DP MX (PS8743B)
	2	
PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

Symbol Note :

 : means Digital Ground

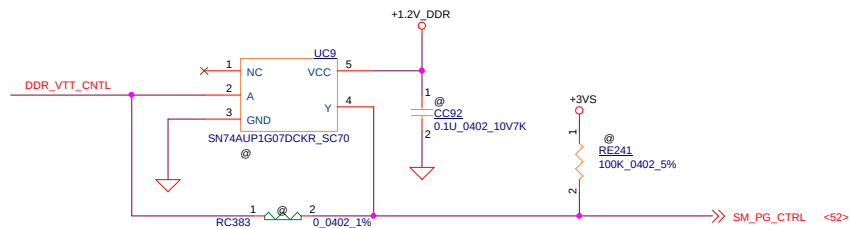
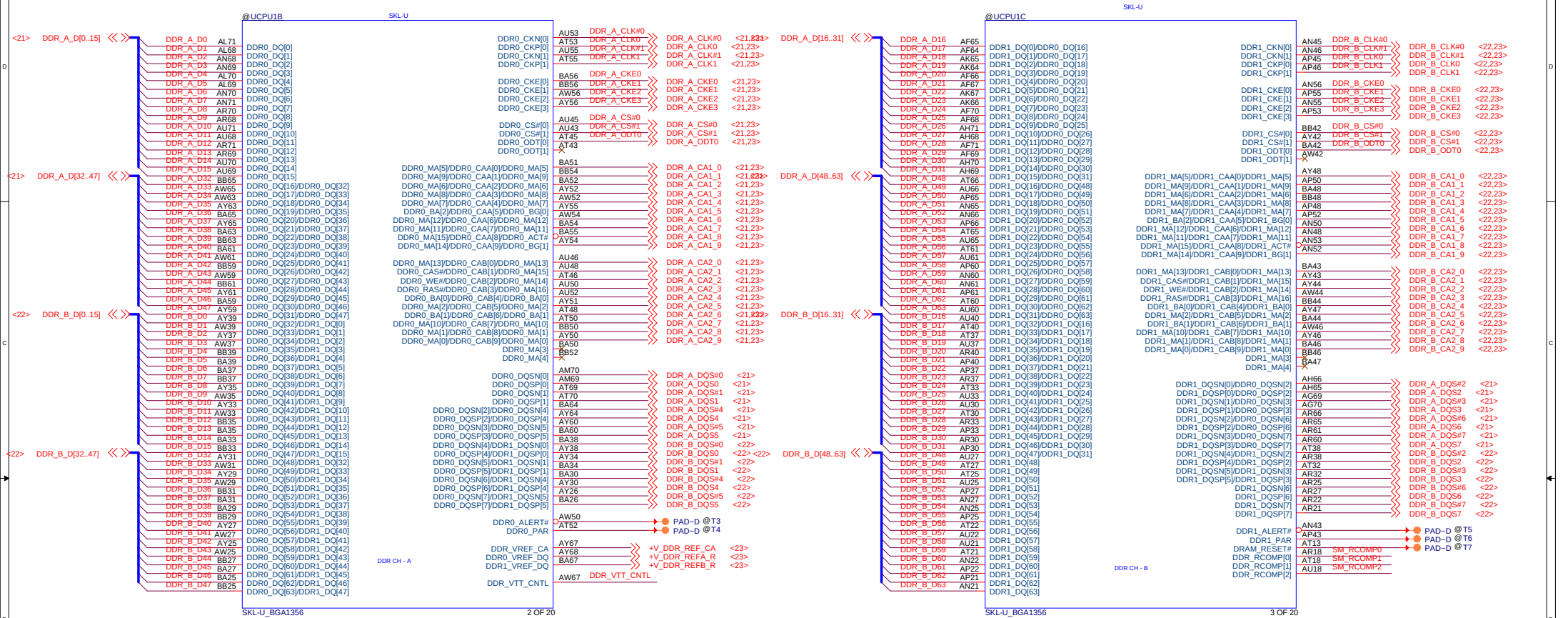
 : means Analog Ground







LPDDR3, Ballout for side by side(Non-Interleave)



LPDDR3 COMPENSATION SIGNALS

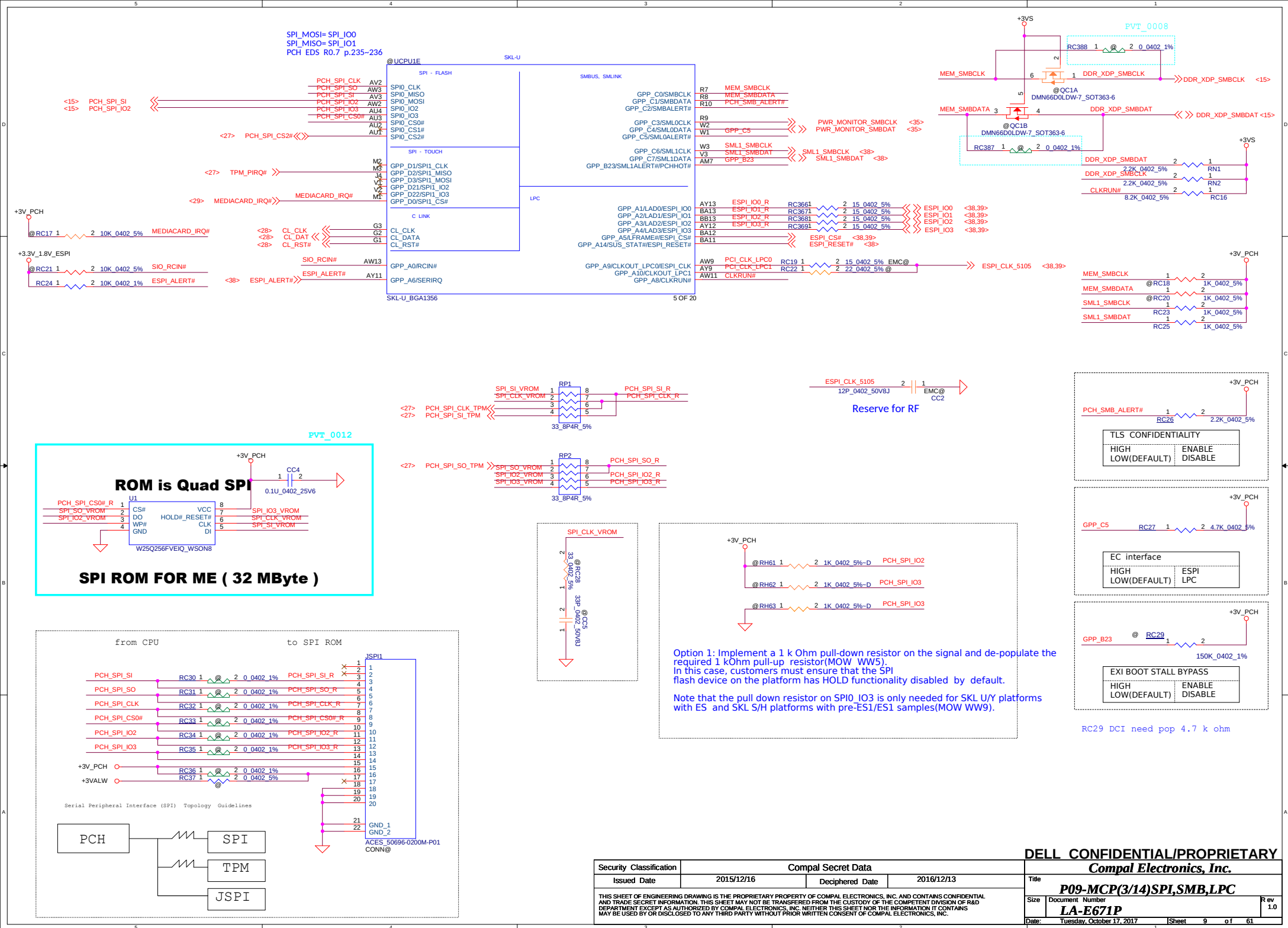


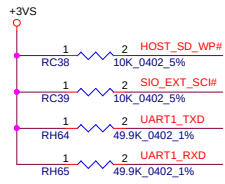
CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Size				Document Number	
LA-E671P				R ev 0.1	
Date: Tuesday, October 17, 2017				Sheet 8 of 61	

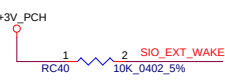
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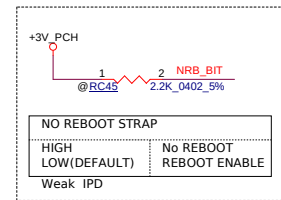
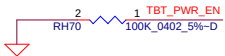




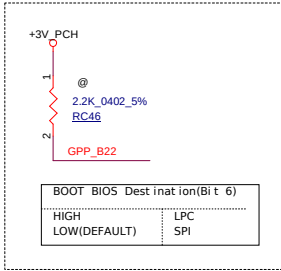
change to net name ==> I2C0_SDA_TS and I2C0_SCK_TS



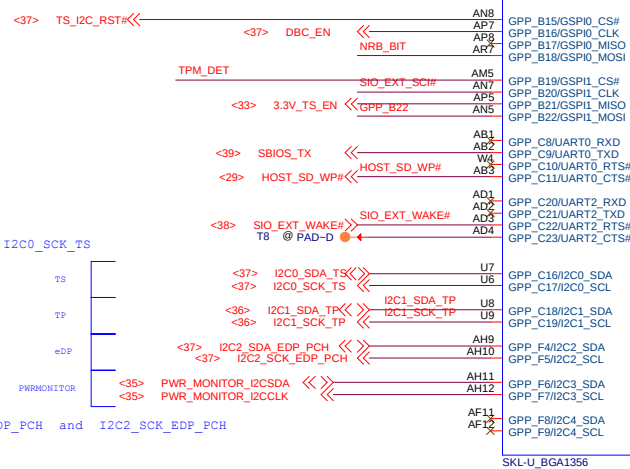
change to net name ==> I2C2_SDA_EDP_PCH and I2C2_SCK_EDP_PCH



NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE
Weak IPD	

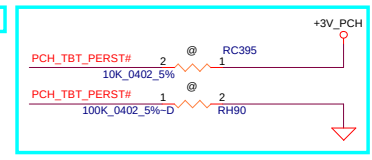
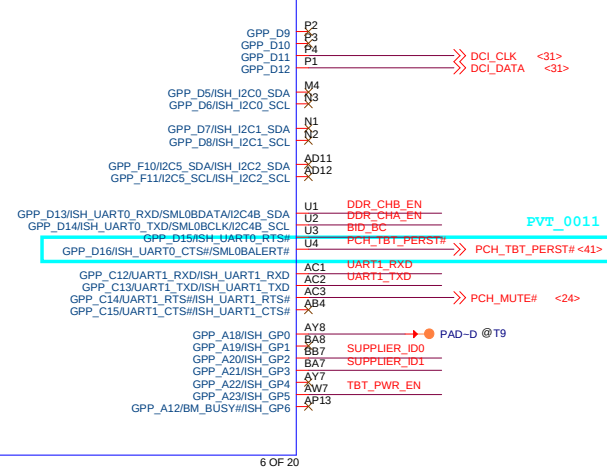
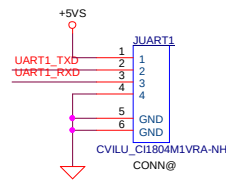


BOOT BIOS Destination (Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

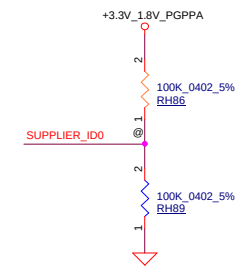
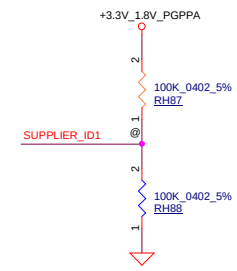
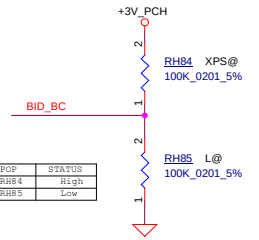


TPM BOM Optional

TPM_DET	
TPM	1 = W/TPM 0 = W/O TPM



Product	POP	STATUS
XPS	RH84	High
L	RH85	Low



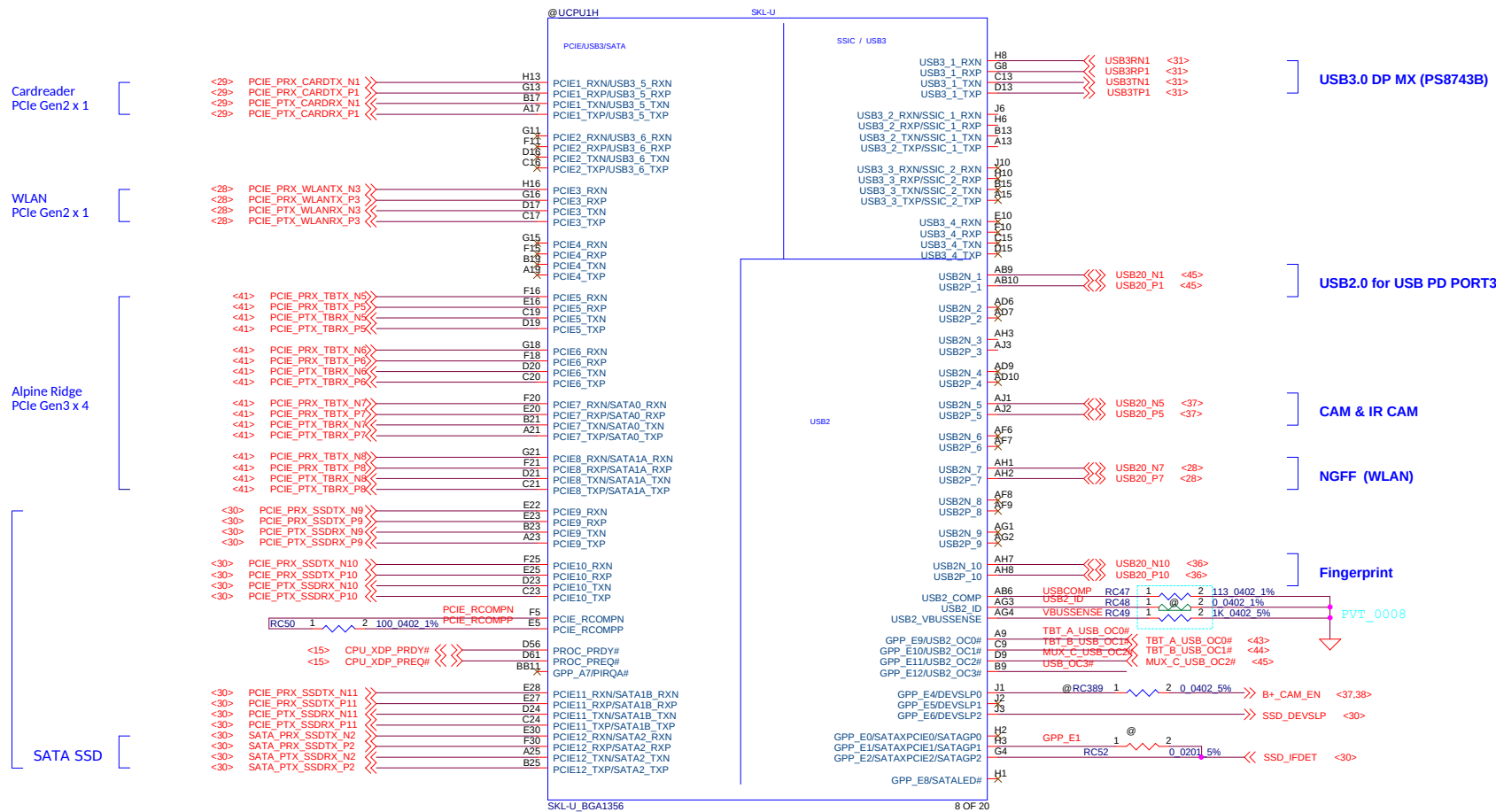
RH87	RH88	RH86	RH89		REV
V	V	V	V	0 0	Supplier A
V	V	V	V	0 1	Supplier B
V	V	V	V	1 0	Supplier C
V	V	V	V	1 1	Supplier D

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Title	P10-MCP(4/14)GSPi,I2C,UART,ISH	
Size	Document	Number
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Date:	Tuesday, October 17, 2017	Sheet 10 of 61



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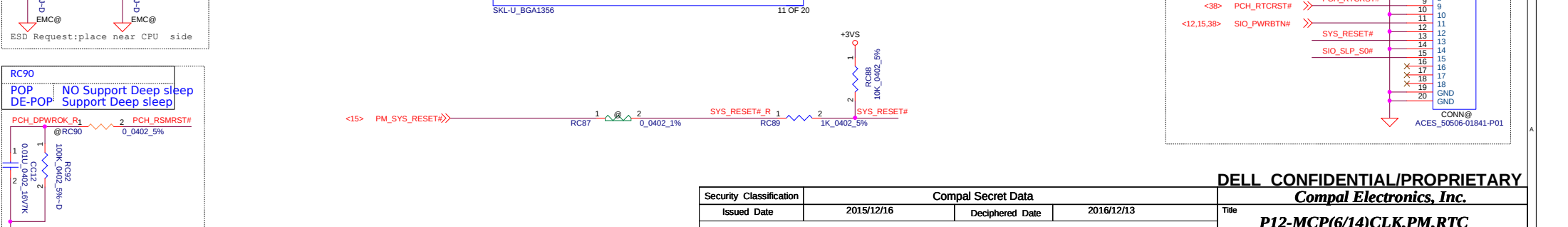
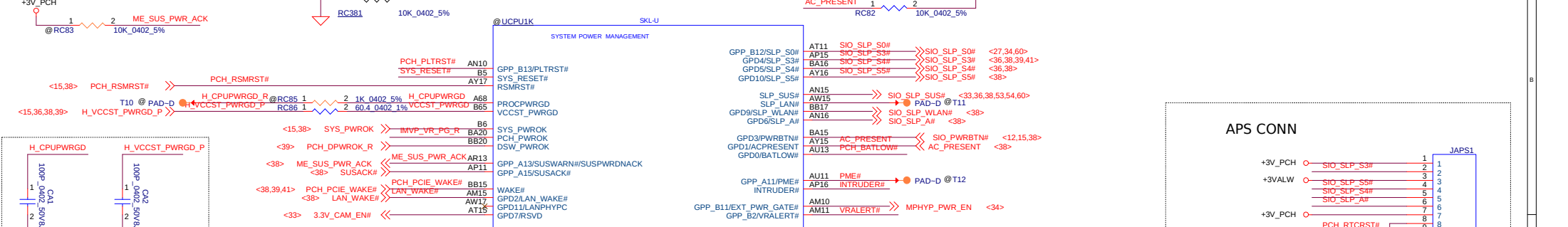
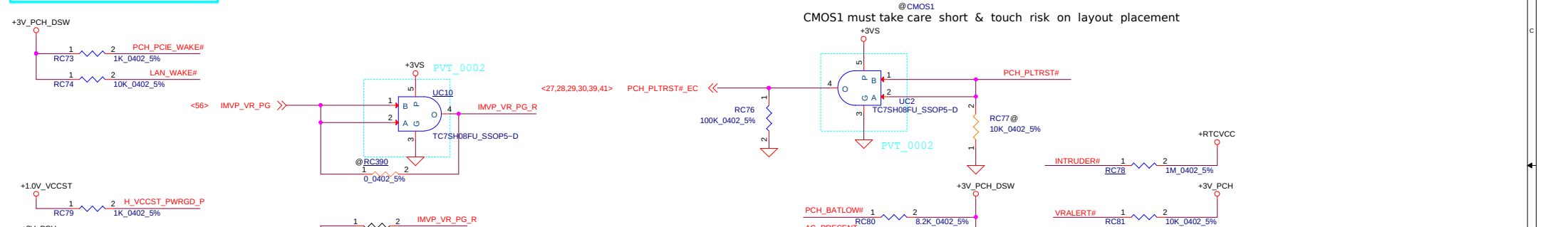
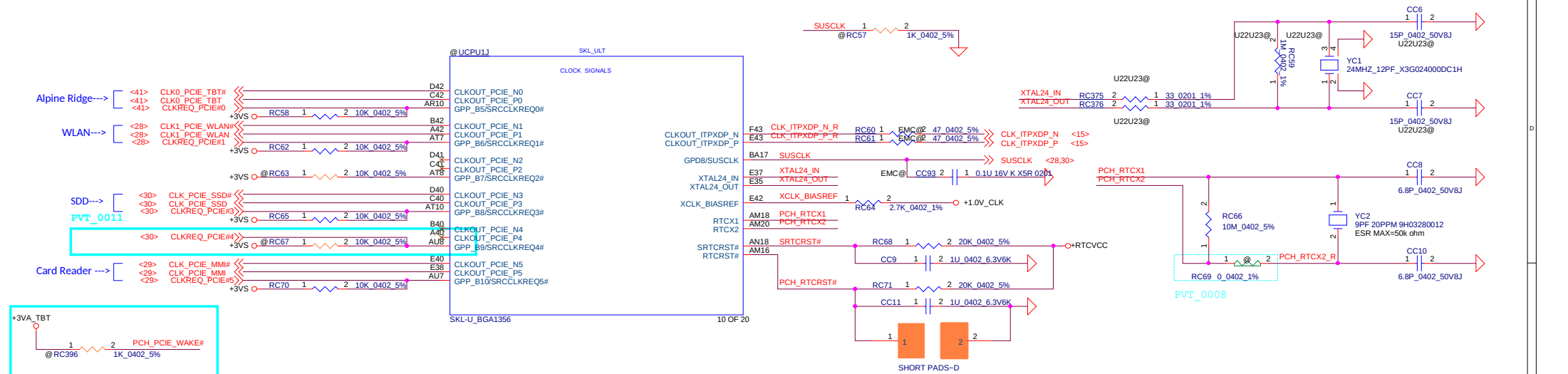
Compal Electronics, Inc.

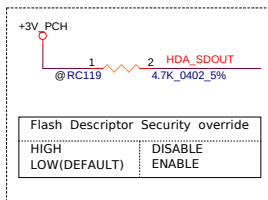
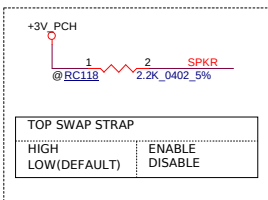
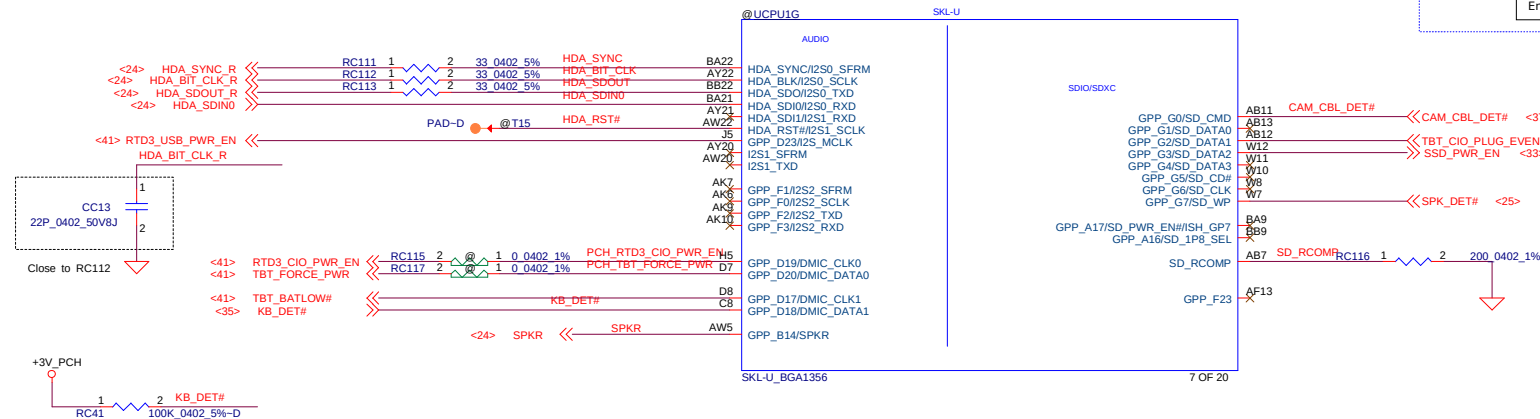
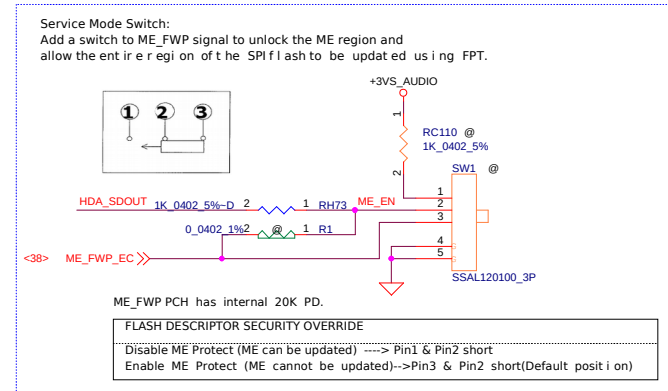
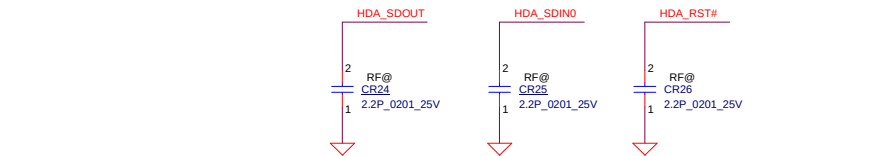
P11-MCP(5/14)PCIE,USB,SATA

LA-E671P

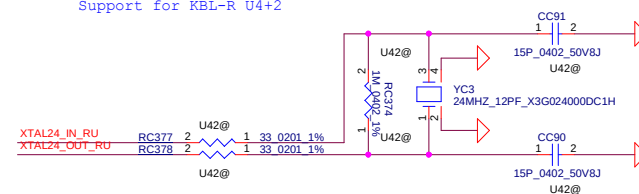
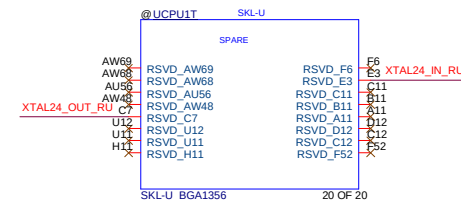
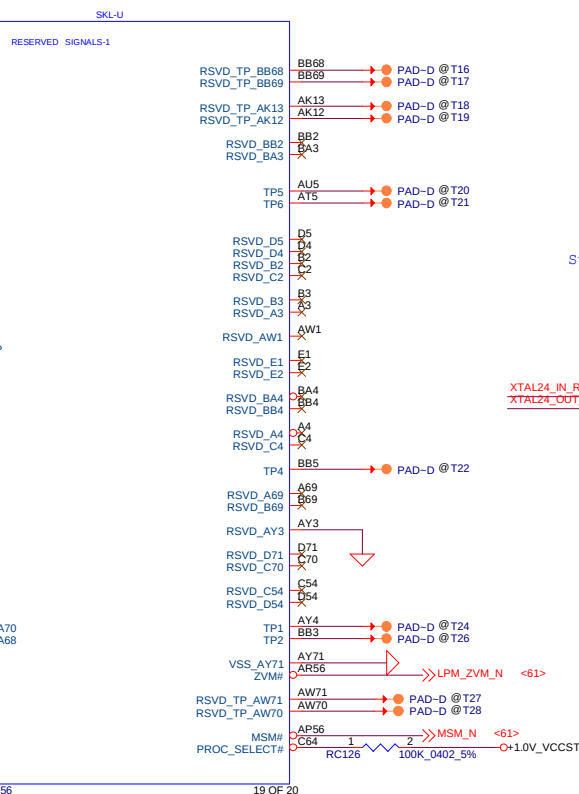
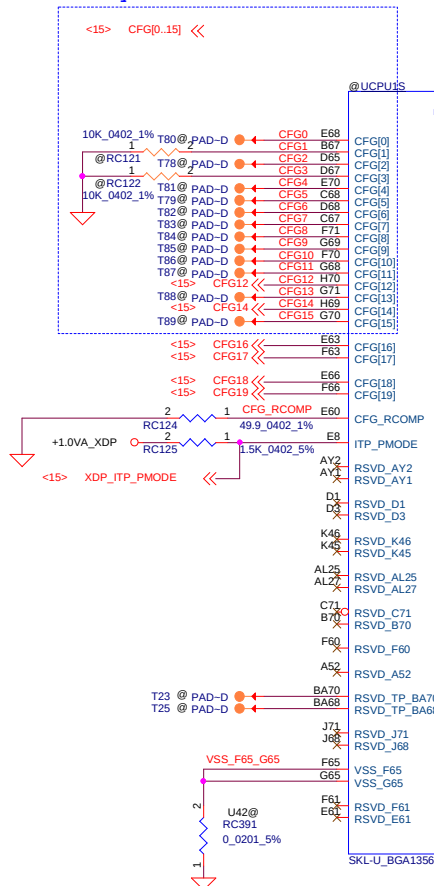
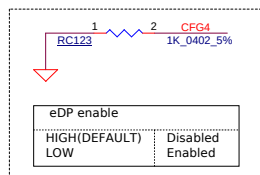
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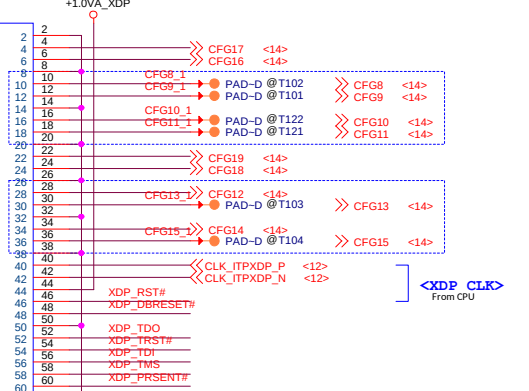
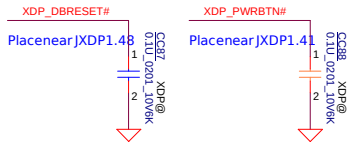




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				Size	Document Number
				LA-E671P	
				Date:	Tuesday, October 17, 2017
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MSM# for SKYLAKE-U 2+3e



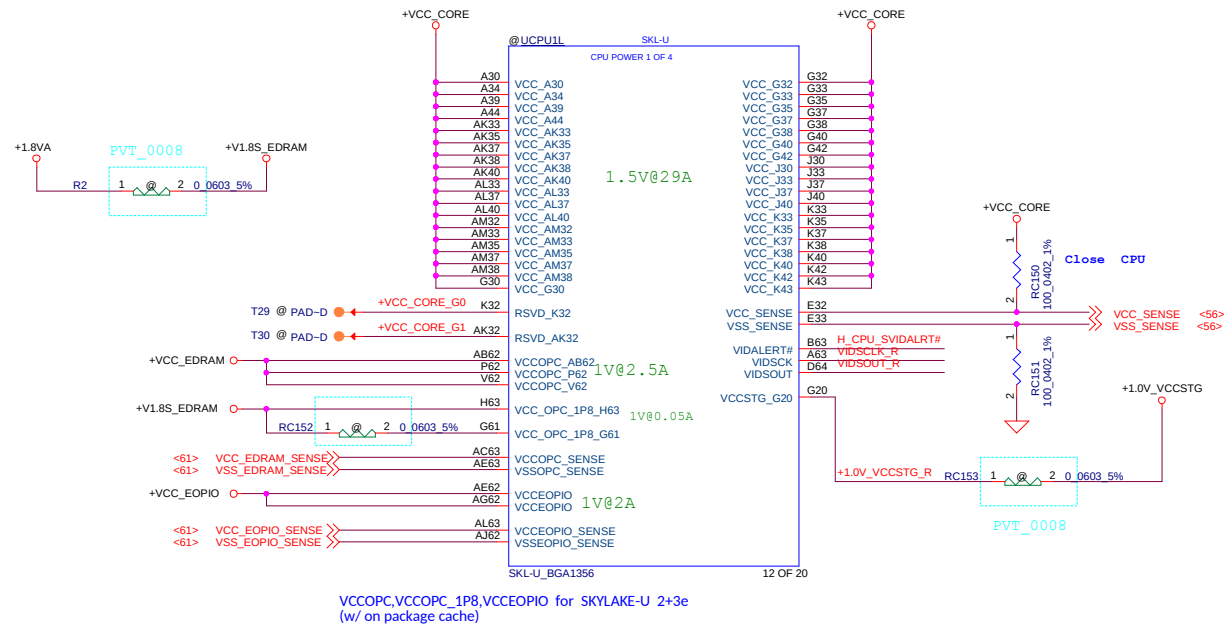
<XDP CLK>
From CPU

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/12/16	Deciphered Date	2016/12/13	Title	P15-MCP(9/14)XDP	
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				Date:	Tuesday, October 17, 2017	Sheet

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

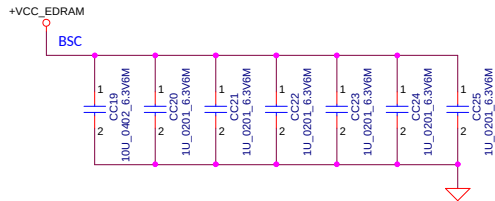
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A

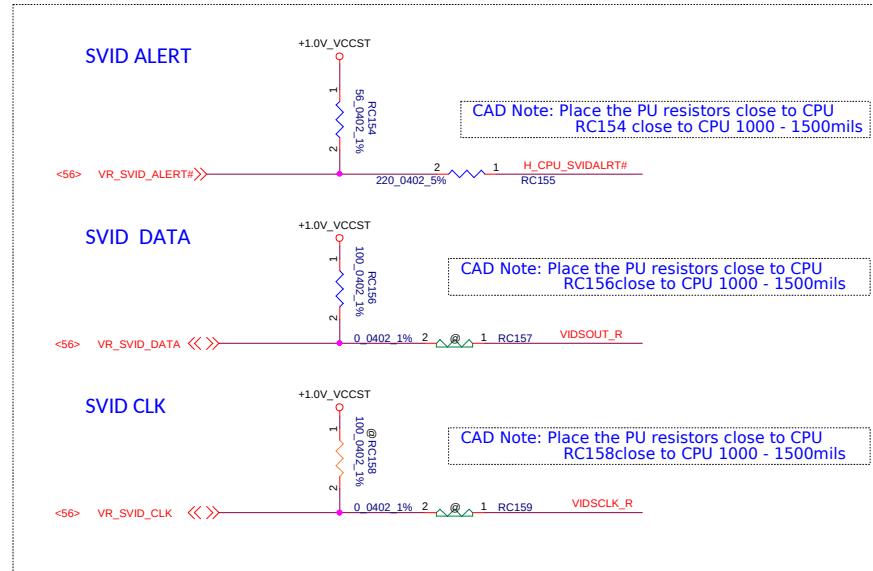
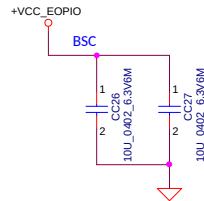


VCCOPC,VCCOPC_1P8,VCCEPIO for SKYLAKE-U 2+3e
(w/ on package cache)

+VCC_EDRAM Decoupling Requirement
Back Side (underneath the package):
10U_0402*1 pcs + 1U_0201*6 pcs



+VCC_EOPIO Decoupling Requirement
Back Side (underneath the package):
10U_0402*2 pcs



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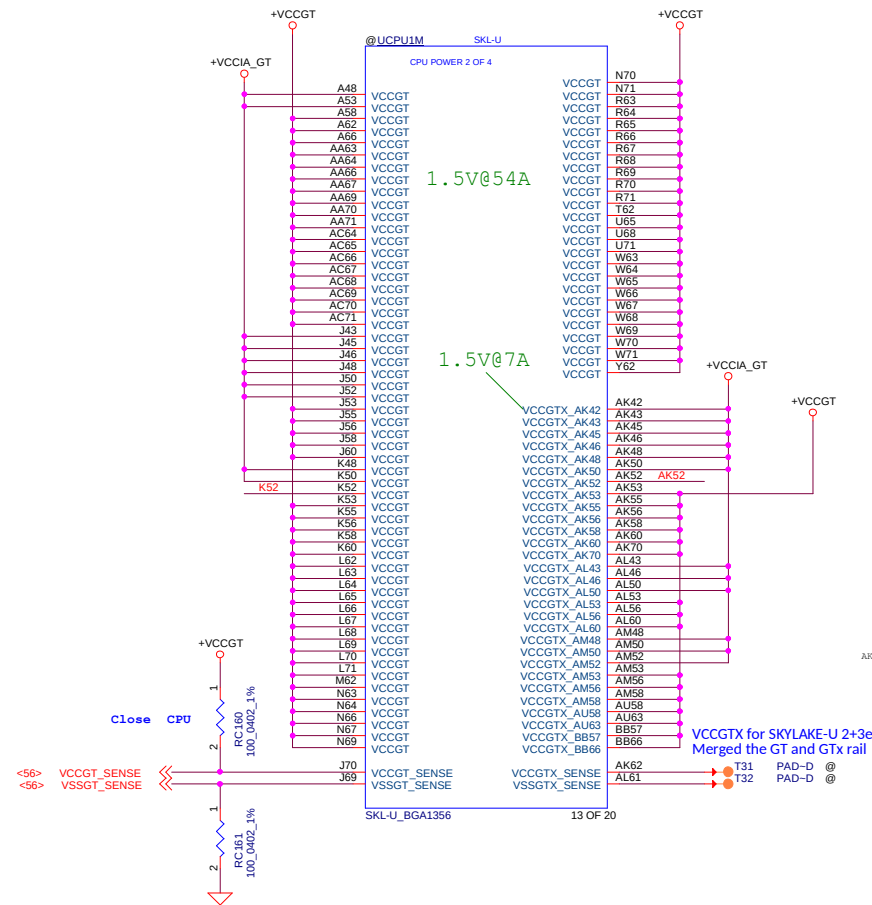
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Issued Date	2015/12/16	Deciphered Date	2016/12/13

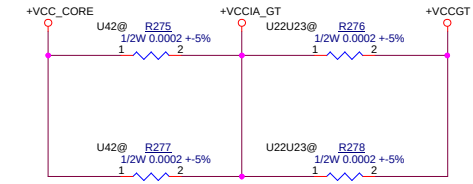
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Computer Electronics, Inc.		
Title		
P16-MCP(10/14)PWR-VCC CORE		
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+VCCGT: 0.55~1.5V, 54A
+VCCGTX: 0.55~1.5V, 7A



Note: 4+2 Co-layout Only can use SD00001VZ00



KBI-R U42 Only Design	Do not Connect AK52 and K52 Bails, Keep as NC
KBI-R U42 Compatible Design for (KBI-R U42/KBI U22/KBI U23e) support	Do not Connect AK52 and K52 Bails, Keep as NC

AK52 and K52 Kaby Lake Silicon Ball Connectivity Recap from PDG (568813_KBL_R_U42_PDG_Addendum_Rev0p9, Page 12)

- VCCGTx for SKYLAKE-U 2+3e
- Merged the GT and GTx rail

T31	PAD-D	@
T32	PAD-D	@

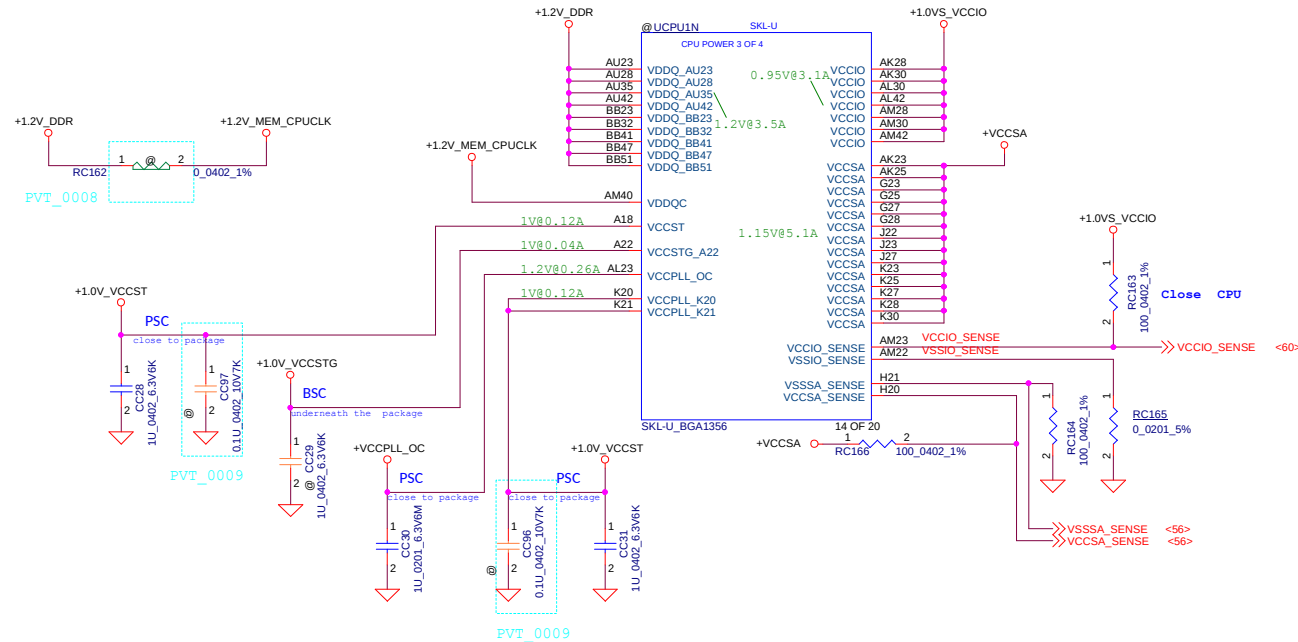
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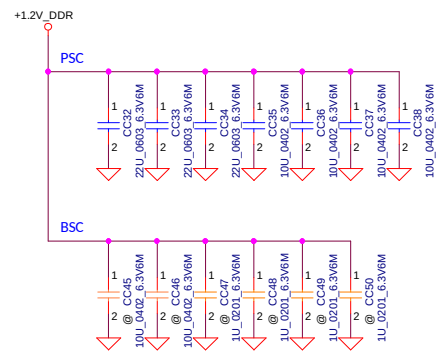
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Issued Date	2015/12/16	Deciphered Date	2016/12/13	<div style="text-align: center;"> CONFIDENTIAL/PROPRIETARY Compal Electronics, Inc. </div>	
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				P17-MCP(11/14)PWR-VCCGT	
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				LA-E671P	
				Date:	Tuesday, October 17, 2017
				Sheet	17 of 61

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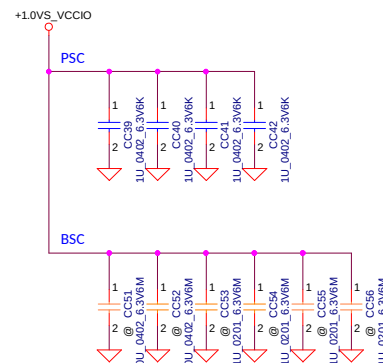
+1.2V_DDR: 1.2V, 3.5A
+1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
+1.0V_VCCSTG: 1V, 40mA
+VCCPLL_OC: 1.2V, 260mA
+1.0VS_VCCIO: 0.85~0.95V, 3.1A
+VCC_SA: 1.15V, 5.1A



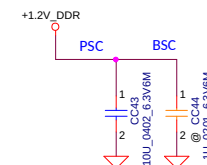
```
+1.2_DDR Decoupling Requirement
Back_Side (underneath the package):
10U_0402*2 pcs + 1U_0201*4 pcs (@)
Primary_Side (close to package):
10U_0402*4 pcs + 22U_0603*3 pcs
```



```
+1.0VS VCCIO Decoupling Requirement
Back Side (underneath the package):
10U_0402*2 pcs + 1U_0201*4 pcs (@)
Primary Side (close to package):
1U_0402*4 pcs
```

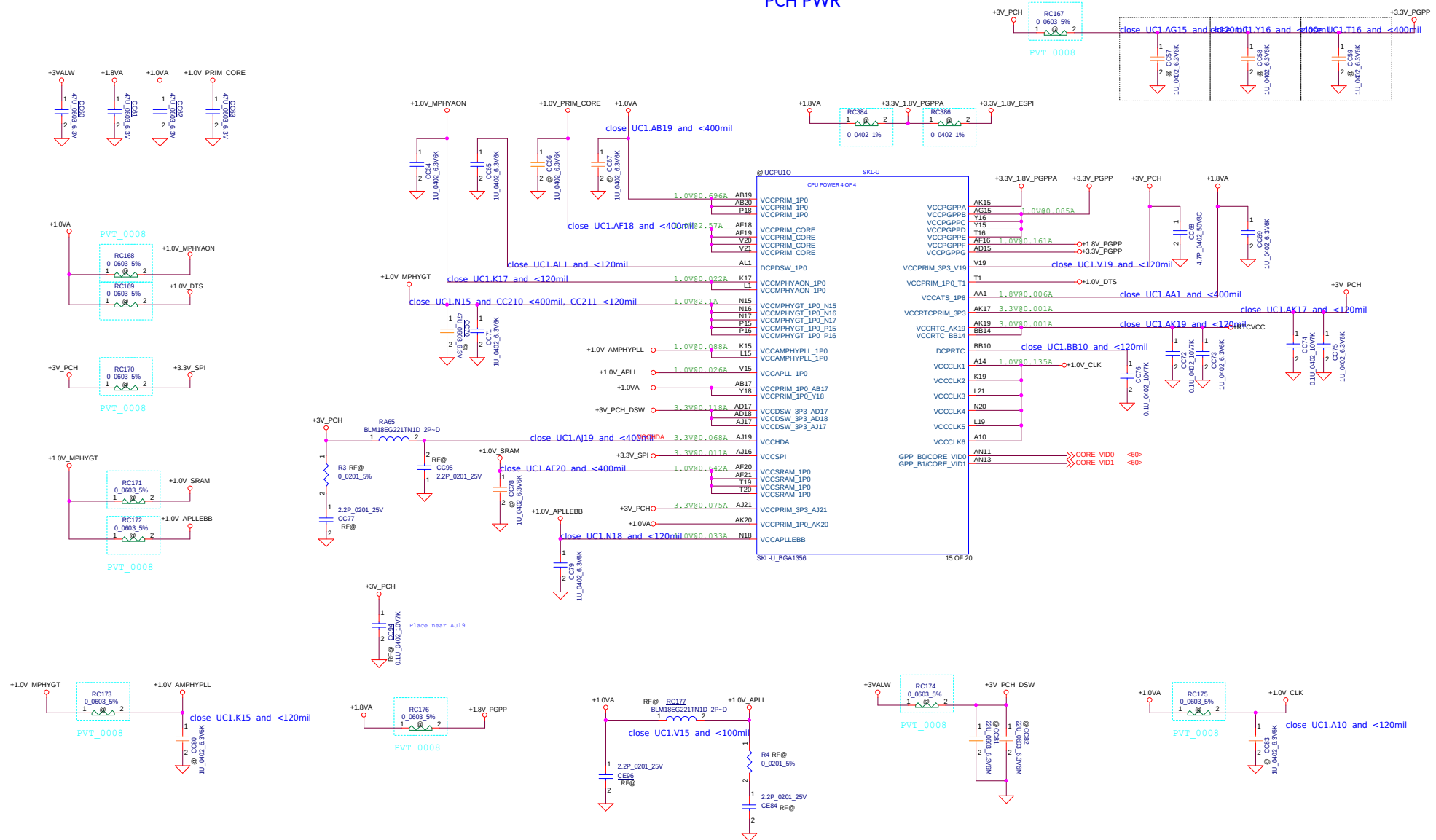


```
+1.2V MEM CPUCCLK (VDDQC) Place on CPU
Back_Side (underneath the package):
1U_0201*1 pcs (@)
Primary Side (close to package):
10U_0402 * 1 pcs
```



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PCH PWR

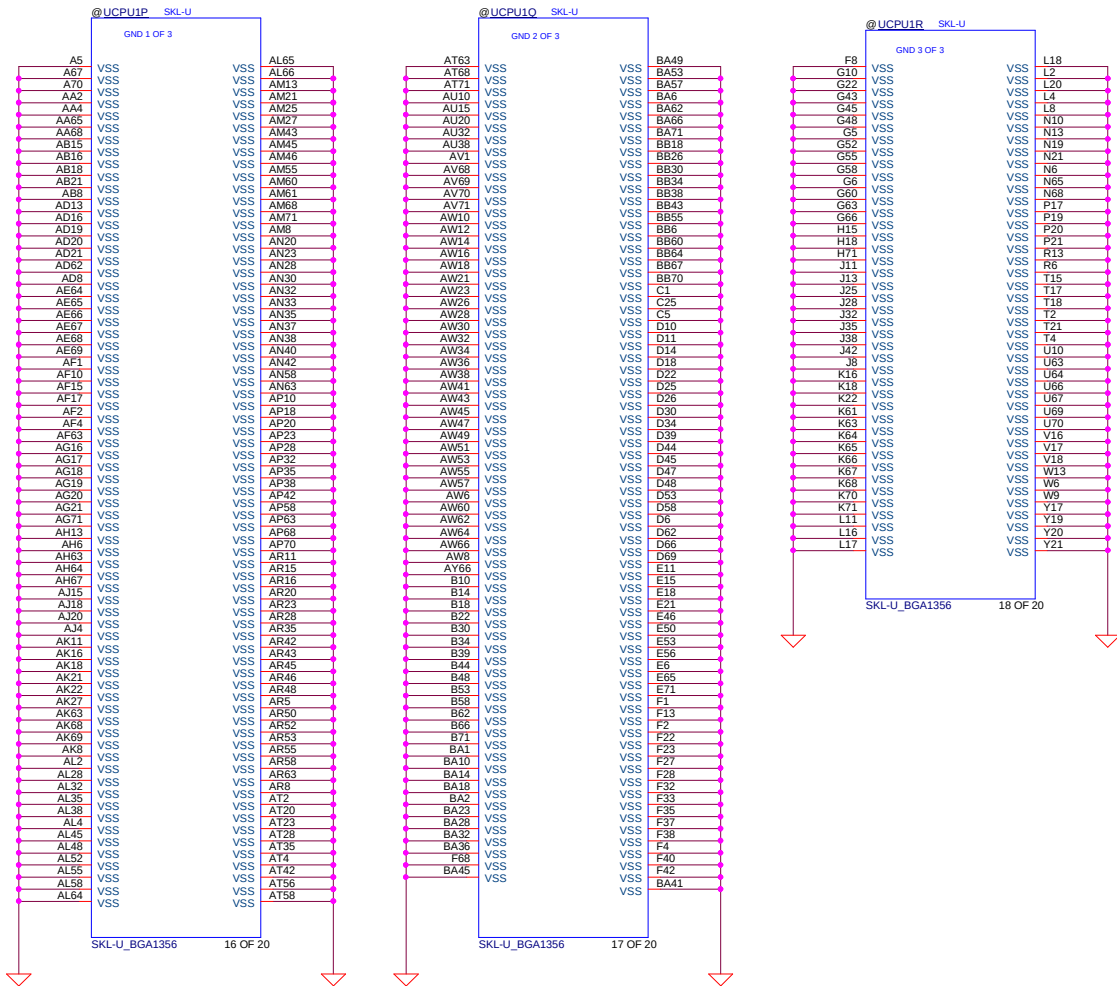


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Title		P19-MCP(13/14)PCH PWR	
Size	Document Number	Rev	
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Date:	Tuesday, October 12, 2017	Sheet	10 of 51

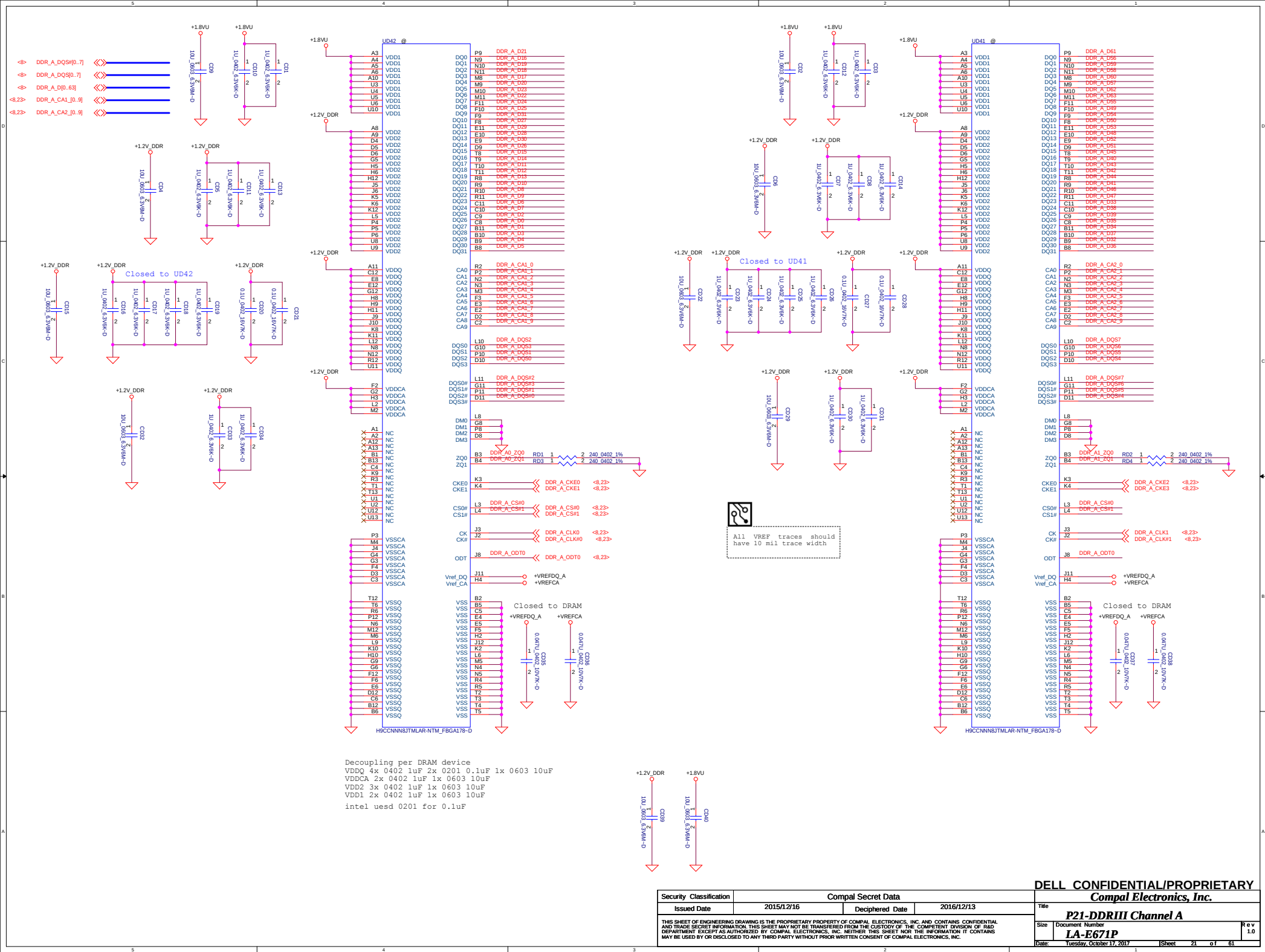
Note1: VCCPRIM_CORE Implementat i on wit hPCH C ORE_VID Rec o mmendat i on

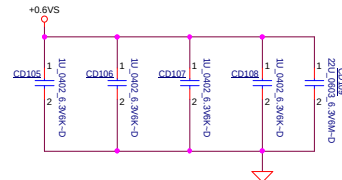
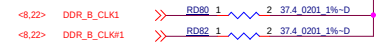
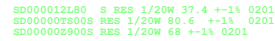
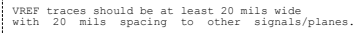


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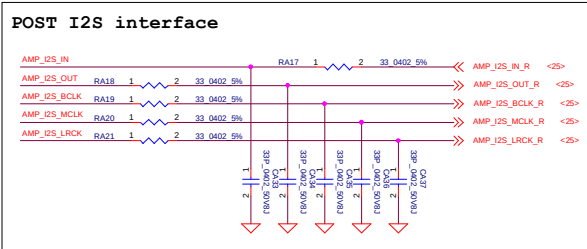
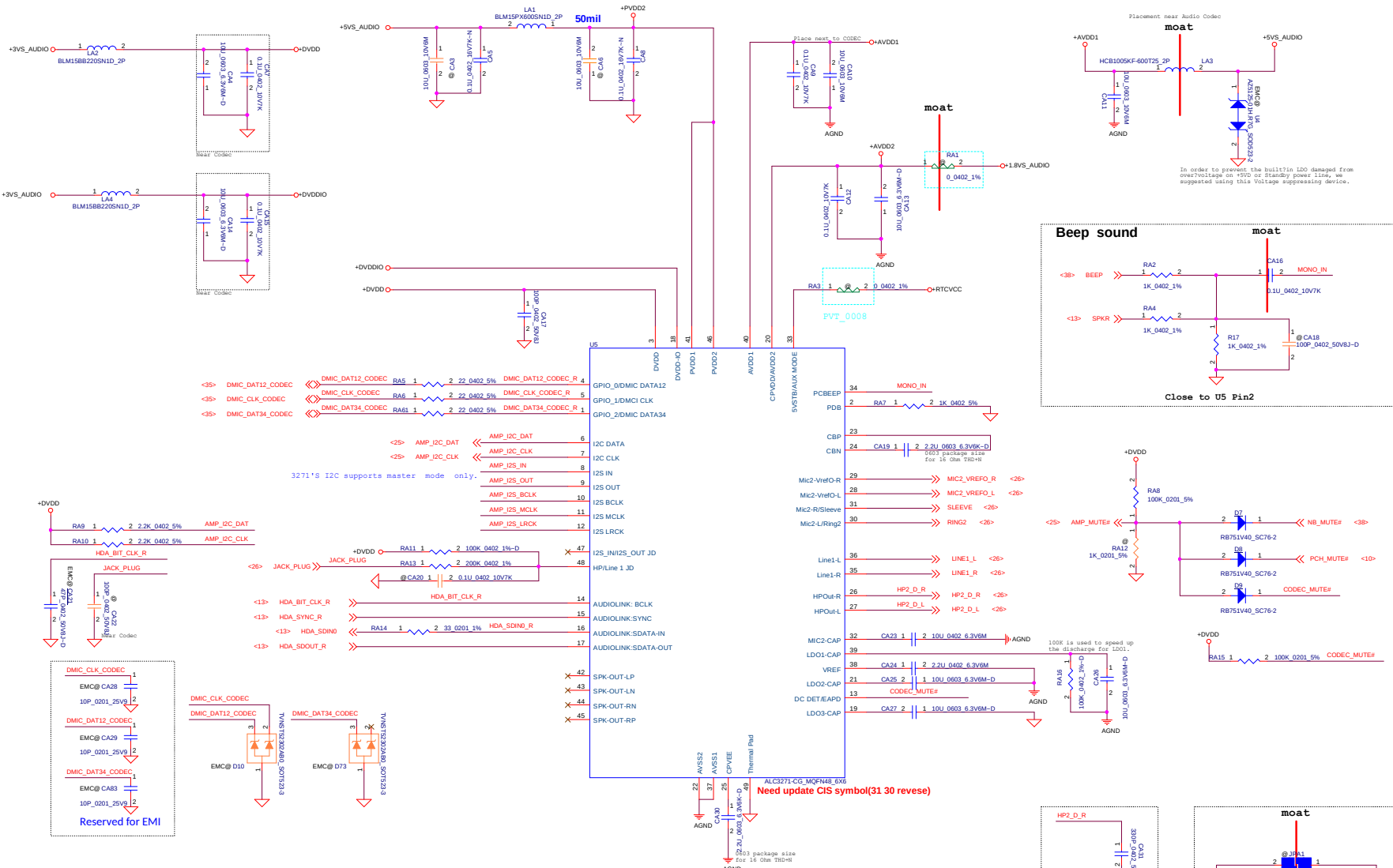
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				Size Document Number
				LA-E671P
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				Rev 1.0





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HD Audio Codec



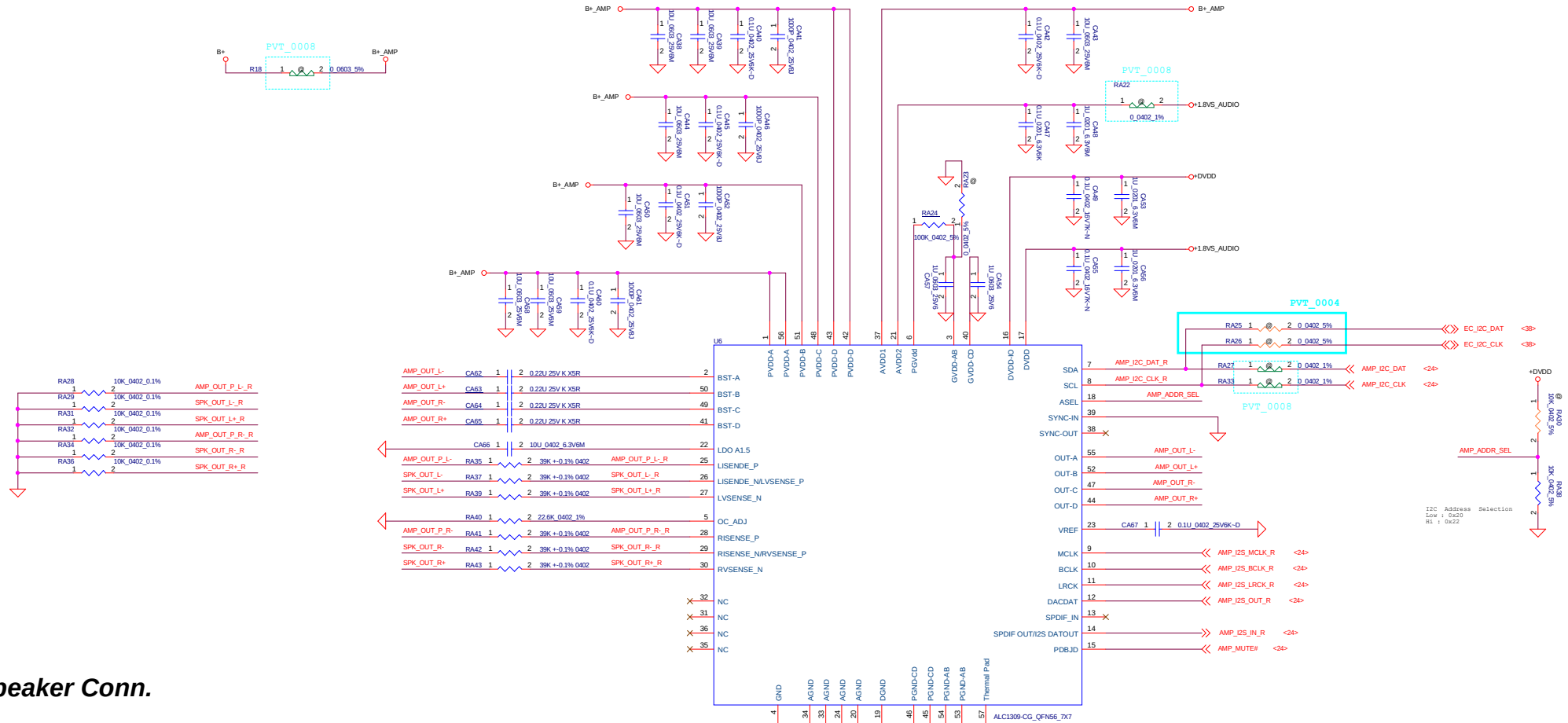
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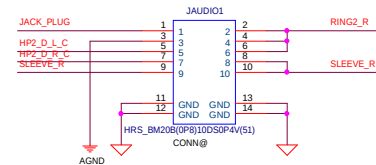
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P24-Audio Codec3271

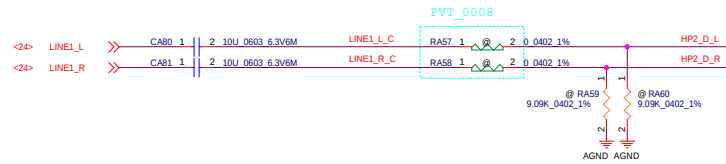
LA-E671P
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SMART AMP





PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.

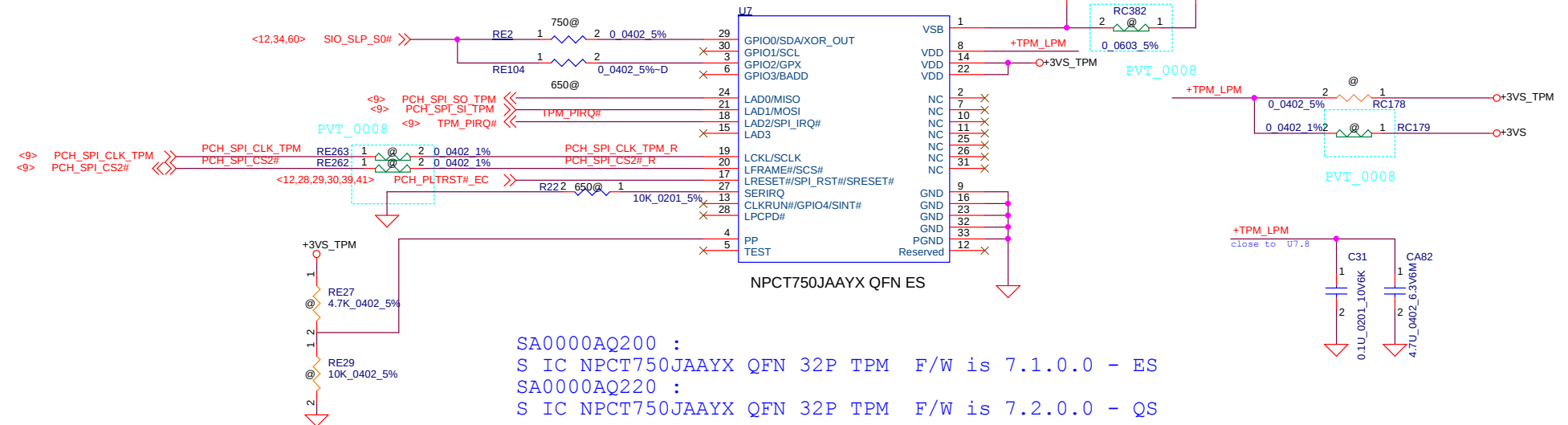
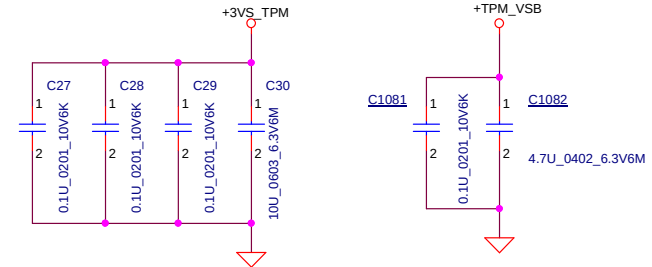
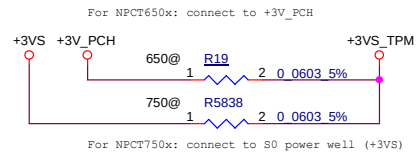


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2041/09/08		2013/10/28		Size Document Number Date: Tuesday, October 17, 2017	
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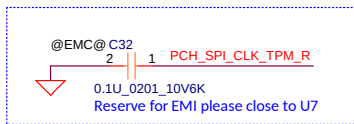
NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide

TPM

NOTE:
Place 0.1 uF capacitors as close as
possible to the device power pins



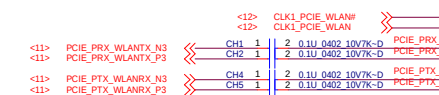
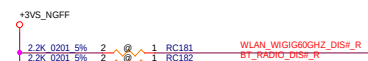
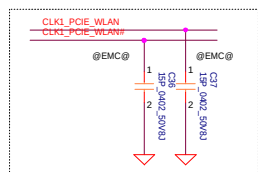
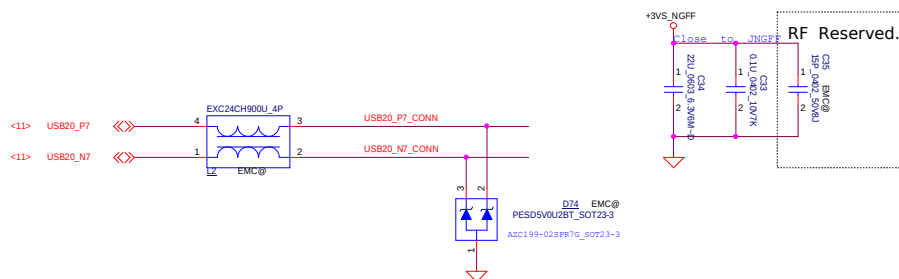
SA0000AQ200 :
S IC NPCT750JAAYX QFN 32P TPM F/W is 7.1.0.0 - ES
SA0000AQ220 :
S IC NPCT750JAAYX QFN 32P TPM F/W is 7.2.0.0 - QS



- Pin14&Pin22 (+3VS_TPM):
For NPCT650x: connect to same power well with host SPI interface (it should be +3V_PCH)
For NPCT750x: connect to S0 power well (+3VS)
- Pin27:
For NPCT650x: pop R22
For NPCT750x: de-pop R22
- SLP S0# connection:
For NPCT650x: pop RE104, de-pop RE2
For NPCT750x: pop RE2, de-pop RE104
- RC180 can be just deleted for both NPCT650x and NPCT750x
- TPM_PIRQ# is recommended that pull-up to same GPIO power well at host side

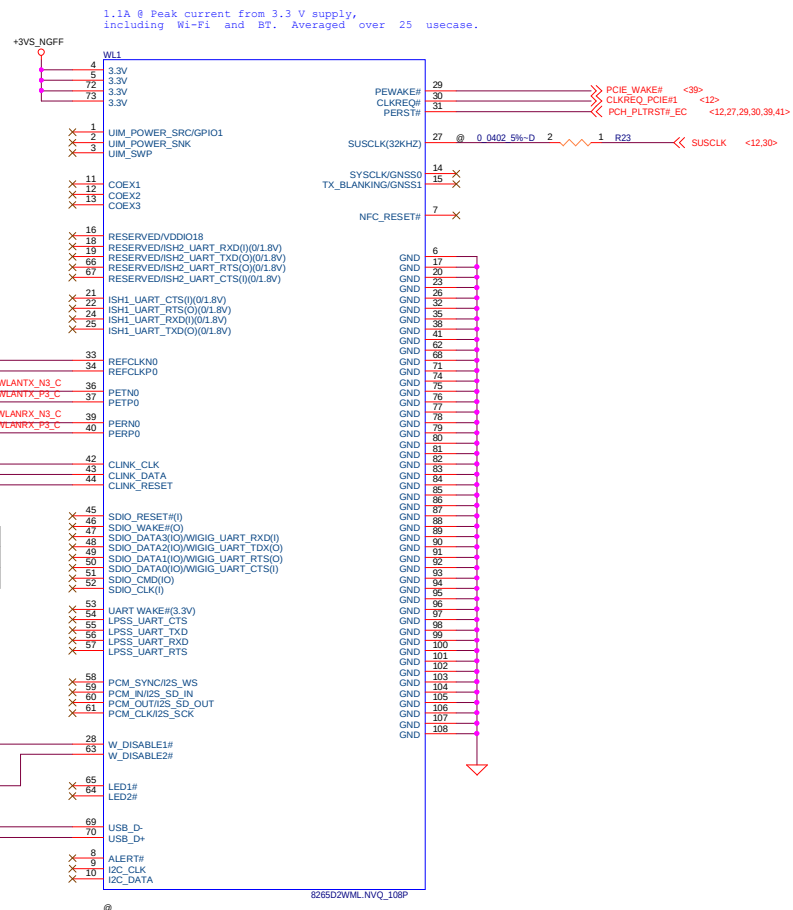
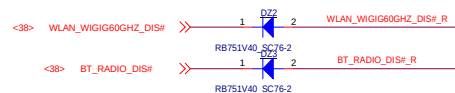
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Issued Date		Deciphered Date		Compal Electronics, Inc.	
2015/12/16		2016/12/13		Title	
				P27-TPM	
				Size	
				Document Number	
				LA-E671P	
				Date	
				Tuesday, October 17, 2017	
				Sheet	
				27 of 61	
				Rev	
				1.0	

M.2 Slot-A Key-A (WLAN)

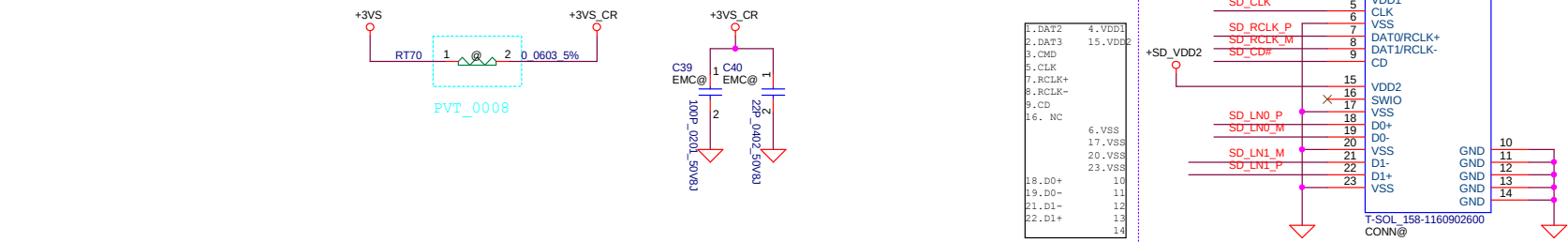


CLINK use for Intel only

Commodity	WLAN	CPN	
Italia XPS	Killer1435-S	PK32000H00L	R24~R26 de-pop
Italia-L	Intel 8265	PK32000GH0L	R24~R26 pop

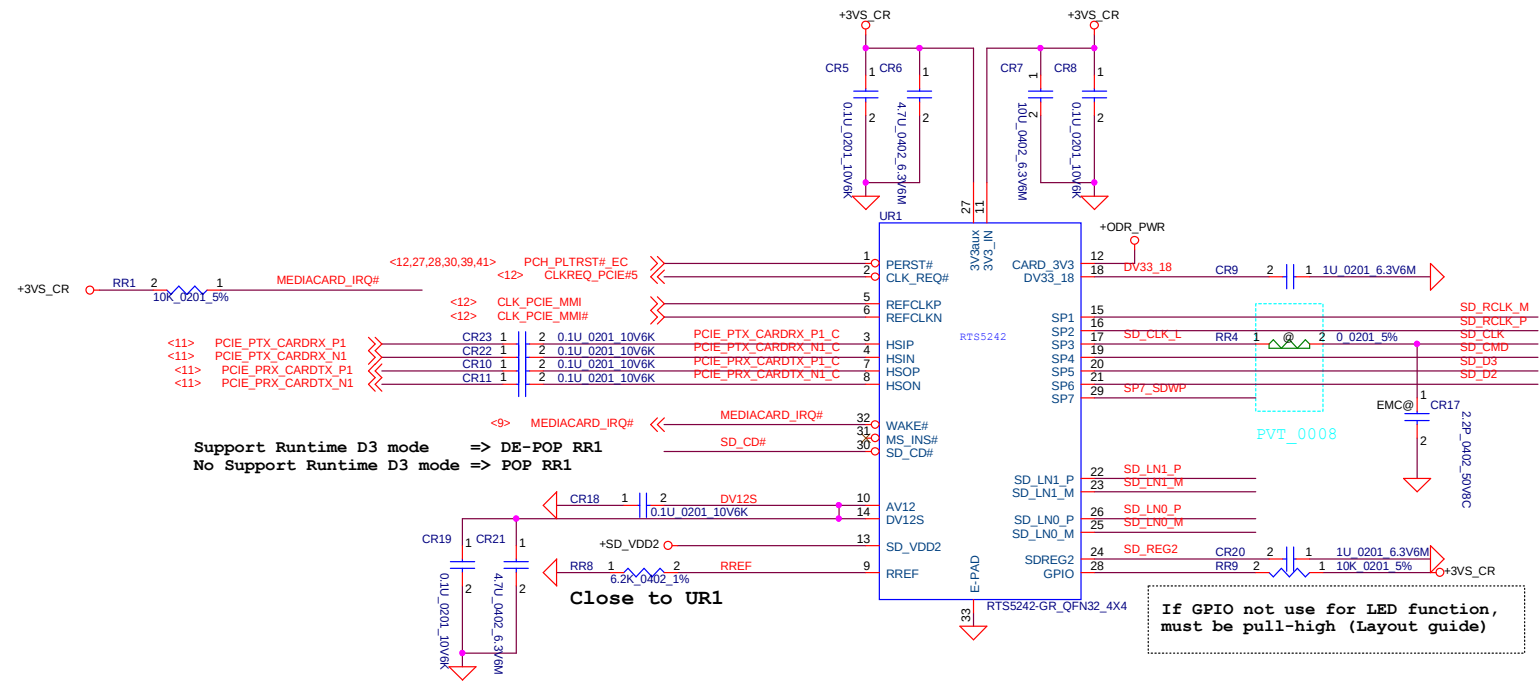


Card Reader

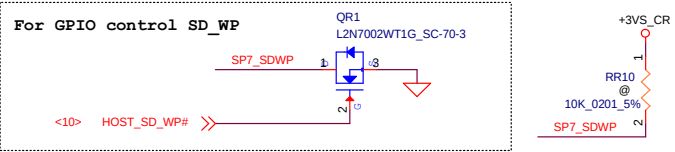


Tom0114:wait CIS symbol
TAISOL 158-1160902600
VDD1=ODR_PWR=3.3V
VDD2=SD_VDD2=1.8V
changed footprint & CPN

Use LTCX007ZY00



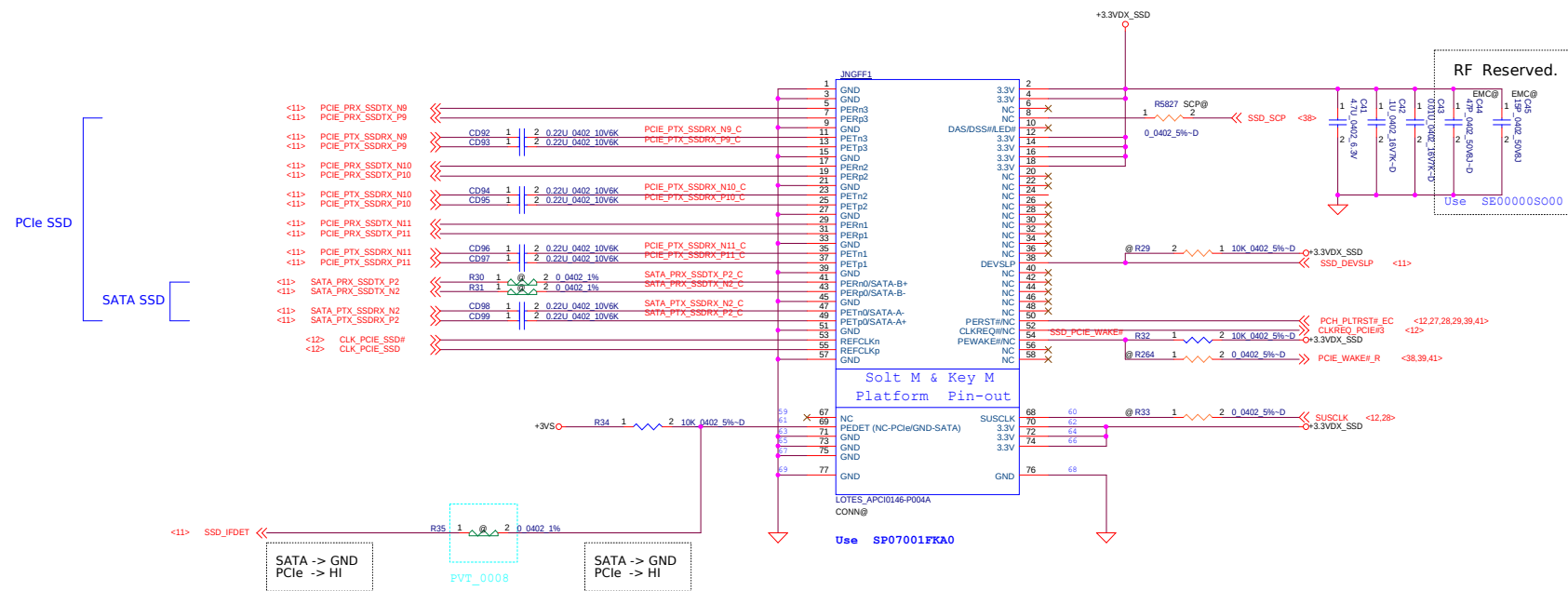
- 1)Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2)Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card 3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3)Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4)Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



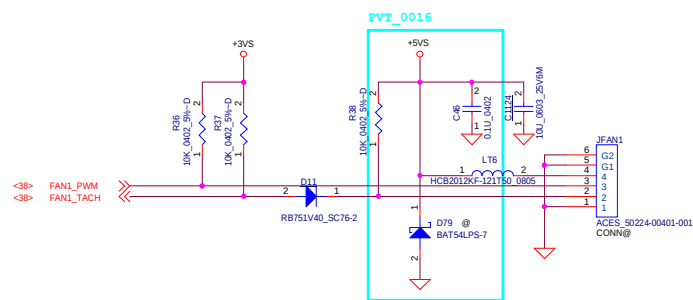
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				LA-E671P	
				Date:	Tuesday, October 17, 2017
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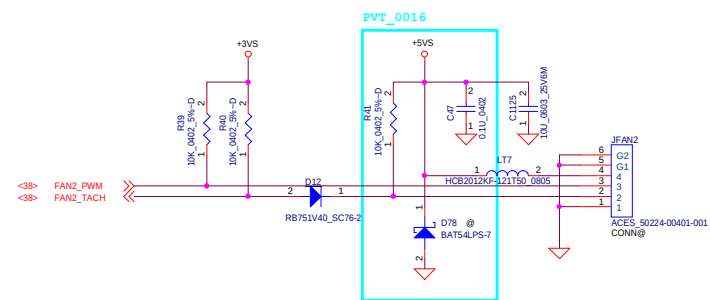
M.2 Slot-C Key-M (SSD)



FAN 1



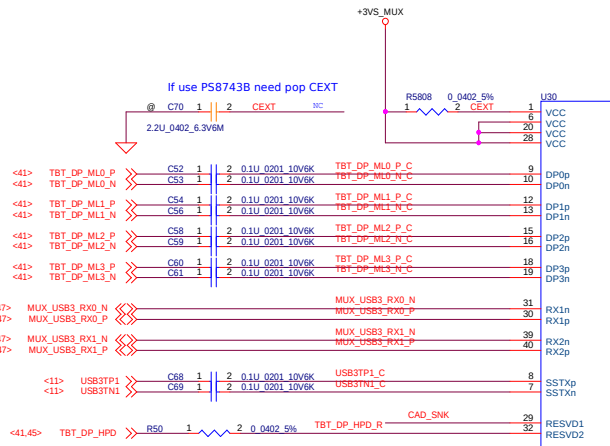
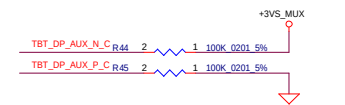
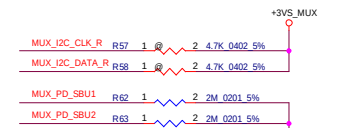
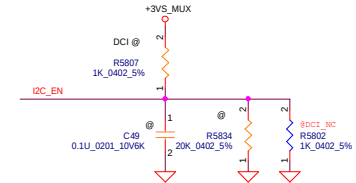
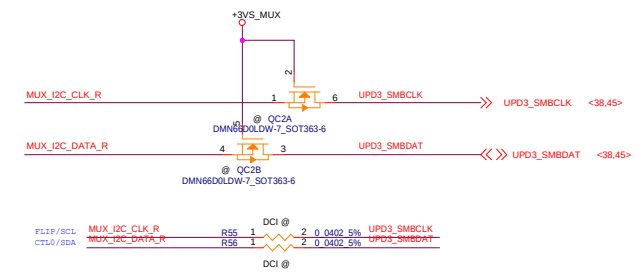
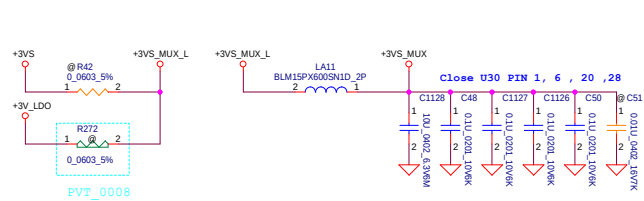
FAN 2



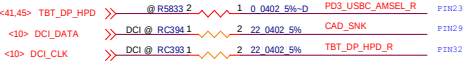
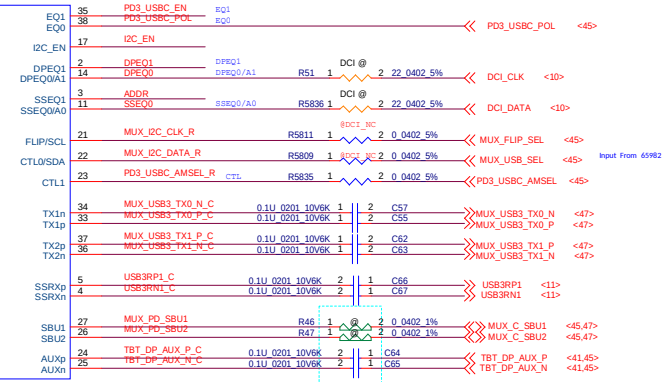
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TUSB546_QFN40_4X6 PVT_0003 PVT_0008
SA00009R720 New CPN for DCI TUSB546A



TI TUSB546 DCI function to add it

PIN	DCI	NON-DCI
23 CTL0/RESPDN	DP ENABLE IN GPIO mode HPD in I2C mode	DP ENABLE IN GPIO mode Unused in I2C mode
29 CAD_SBU1/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

- Bring up summary
1. DCI Tools : Frequency HostConfig.xml file change to Clk133MHz = 2
 2. EC updated TUSB546 reg[0x0A] bit 4 for EQ controlled by I2C.
 3. Pop DCI @ HW parts and Depop @ DCI_NC / PCH RC29 up to 4.7K ohm
 4. For DCI BIOS

LEVEL	SETTINGS
0	Option 1: Tie 1K ohm 5% to GND Option 2: Tie directly to GND
R	Tie 20K ohm 5% to GND
F	Float (leave pin open)
1	Option 1: Tie 1K ohm 5% to VCC Option 2: Tie directly to VCC

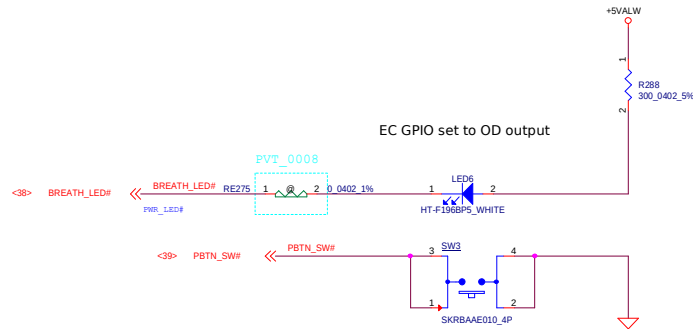
TUSB546 MUX default H/W setting

CTL1 EN (Pin 23)	CTL0 AMSEL (Pin 29)	FLIP PCH (Pin 21)	TUSB546 Configuration	VESA DisplayPort Alt Mode (DP1.2) Configuration
L	L	L	Power Down	
L	L	H	Power Down	
L	H	L	One Port USB 3.1 - No Flap	
L	H	H	One Port USB 3.1 - With Flap	
H	L	L	4 Lane DP - No Flap	C and E
H	L	H	4 Lane DP - With Flap	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flap	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flap	D and F

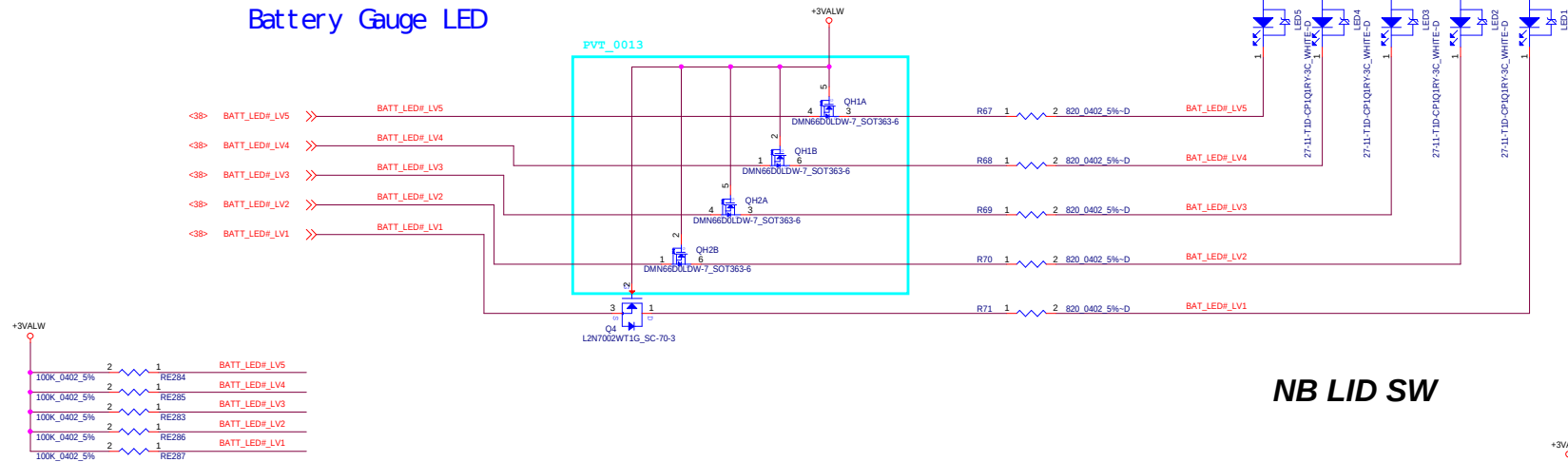
Device Configuration in GPIO Mode

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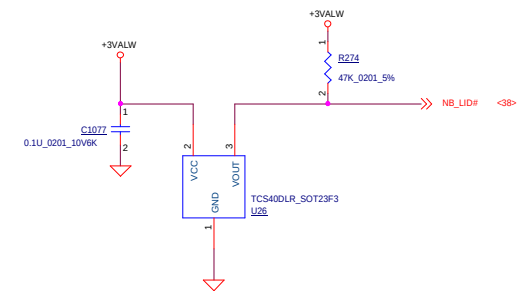
Power Button +LED



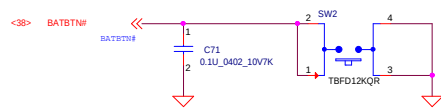
Battery Gauge LED



NB LID SW

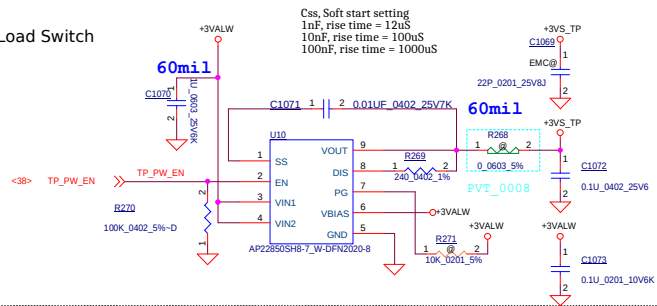


Battery Gauge Button

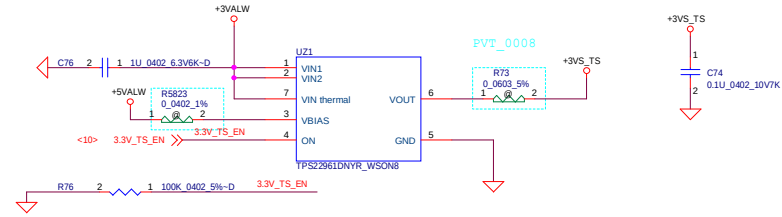


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				P32-Battery LED / LID	
				Size	
				LA-E671P	
				Rev	
				1.0	
				Date	
				Tuesday, October 17, 2017	
				Sheet	
				32 of 61	

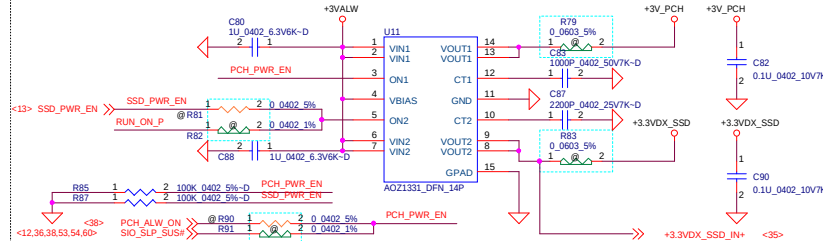
Touch Pad Load Switch



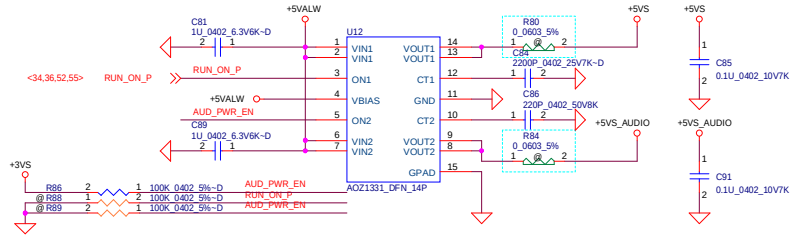
Touch Screen Load Switch



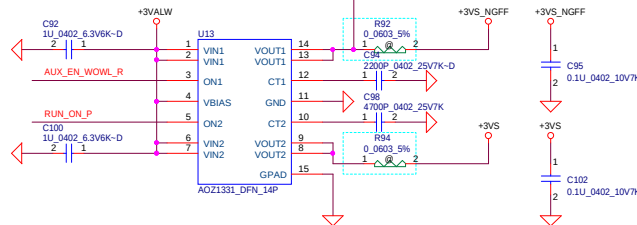
Deeper Sleep, SSD Load Switch



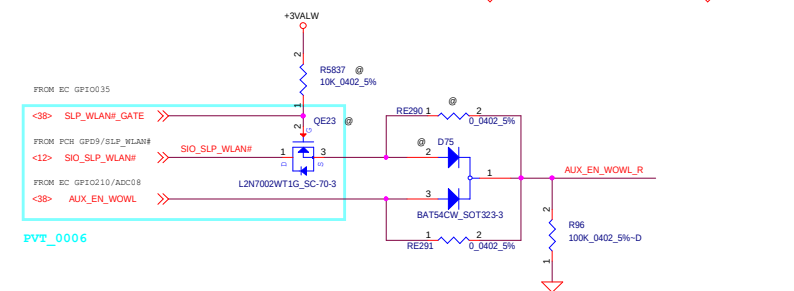
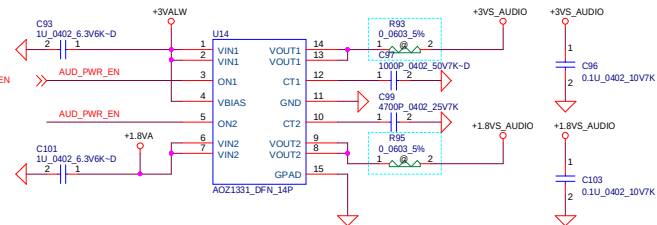
5V_Run, 5V_Audio Load Switch



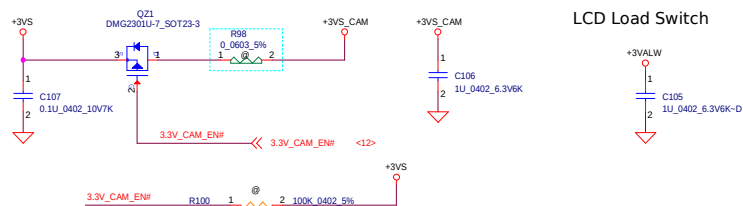
WiFi, 3V_RUN Load Switch



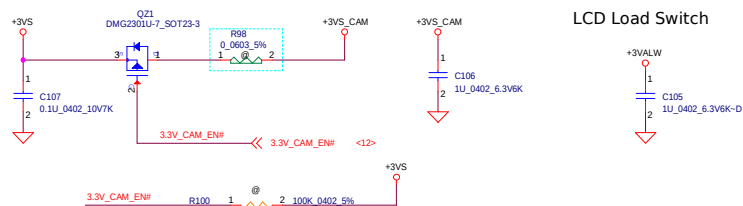
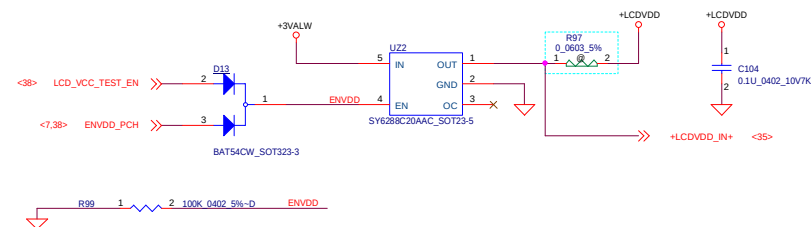
3V_Audio, 1.8V_Audio Load Switch



Camera

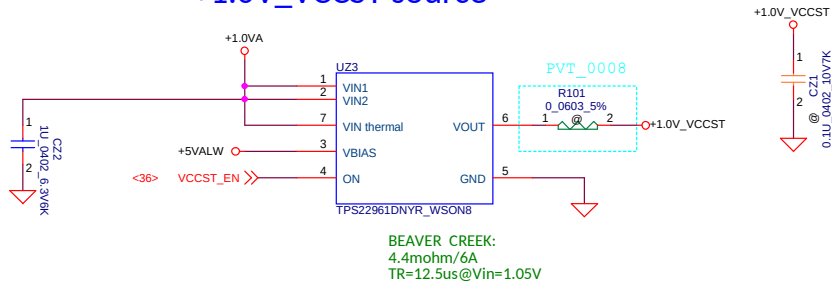


LCD Load Switch

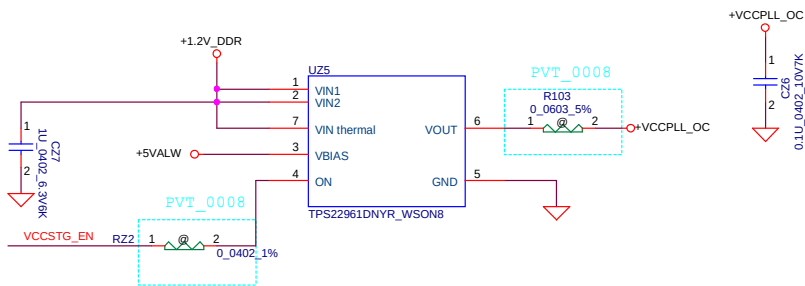


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				Document Number LA-E671P	1.0
Date:		Tuesdays, October 17, 2017		Sheet	33 of 61

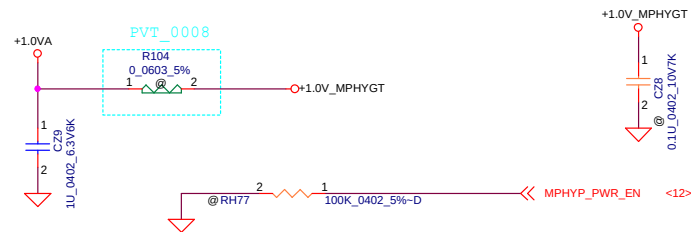
+1.0V_VCCST source



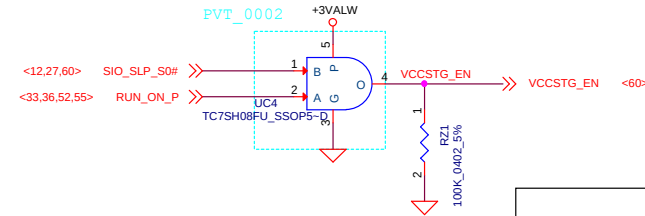
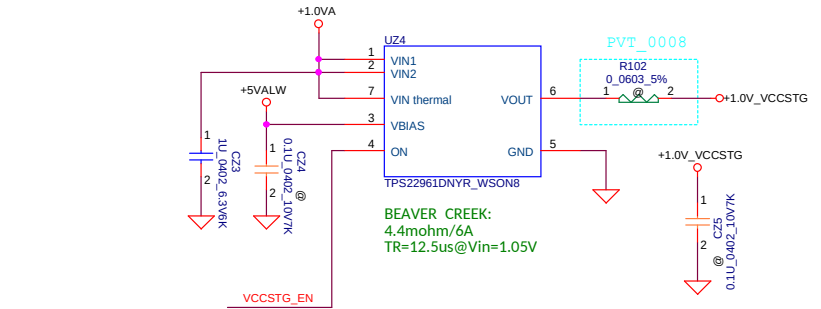
+VCCPLL_OC source



+1.0V_MPHYGT source



+1.0V_VCCSTG source



	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

1



1



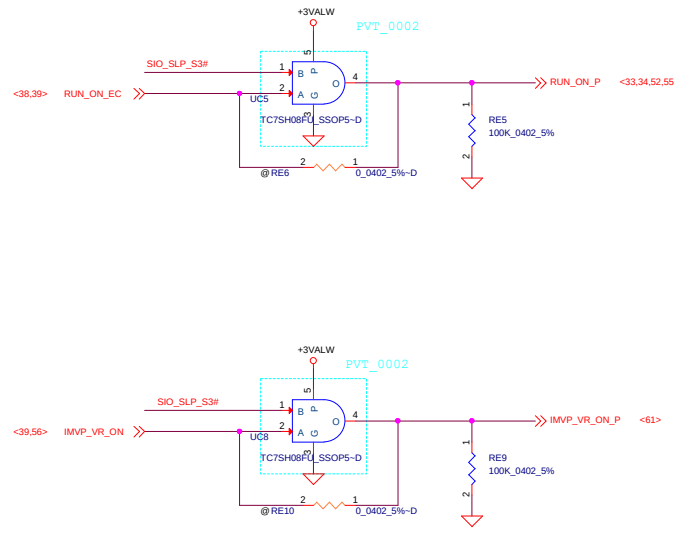
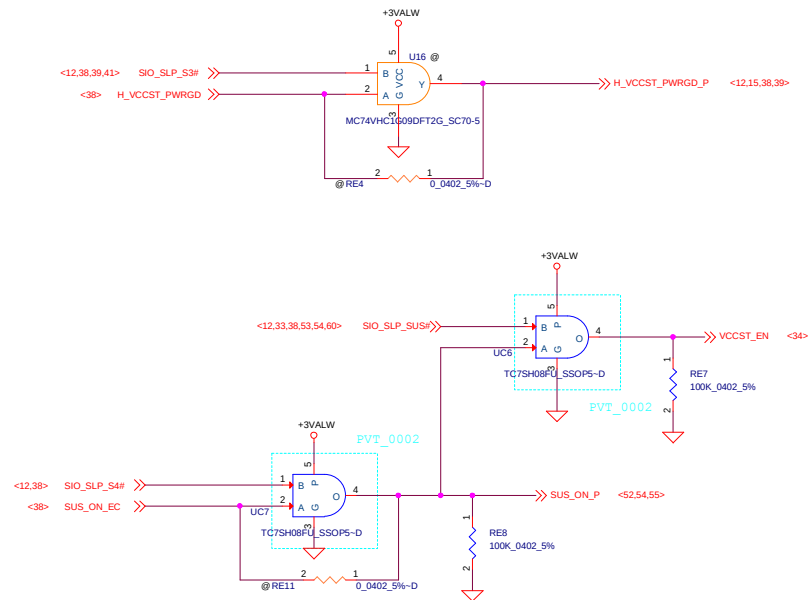
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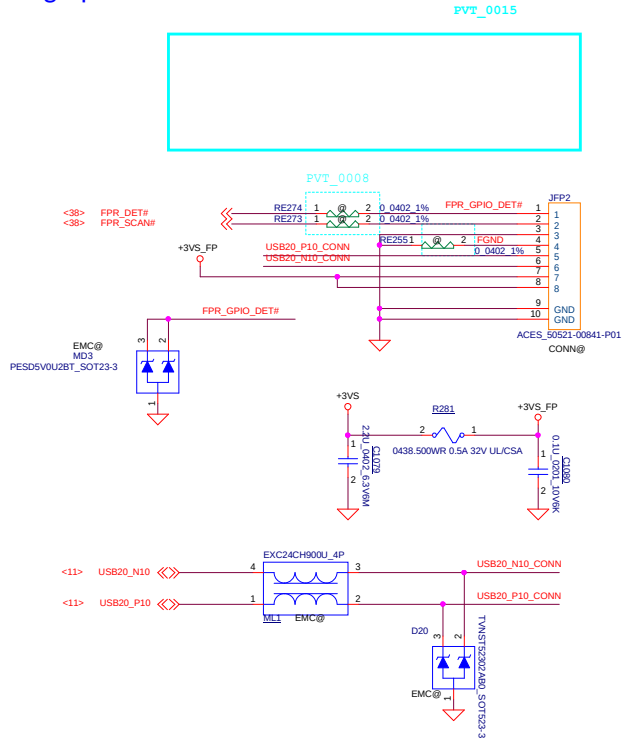
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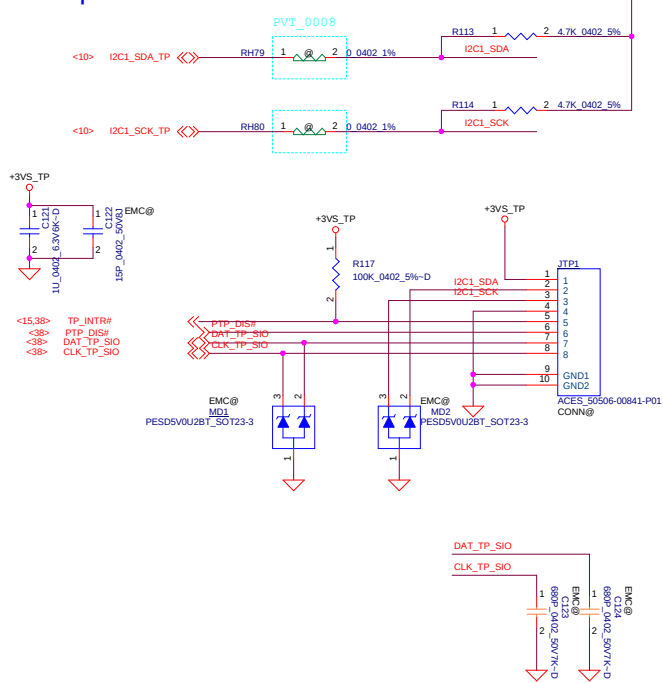
A	B	C	D	E
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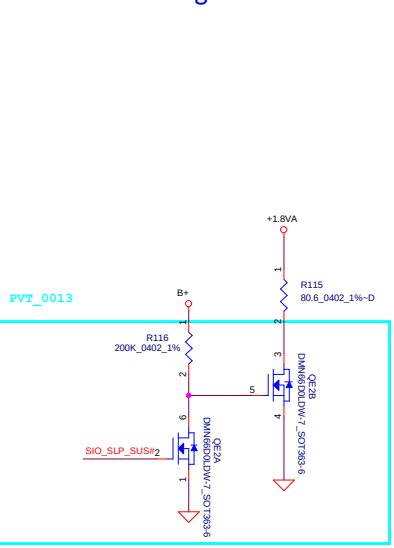
Fingerprint CONN



Touchpad CONN

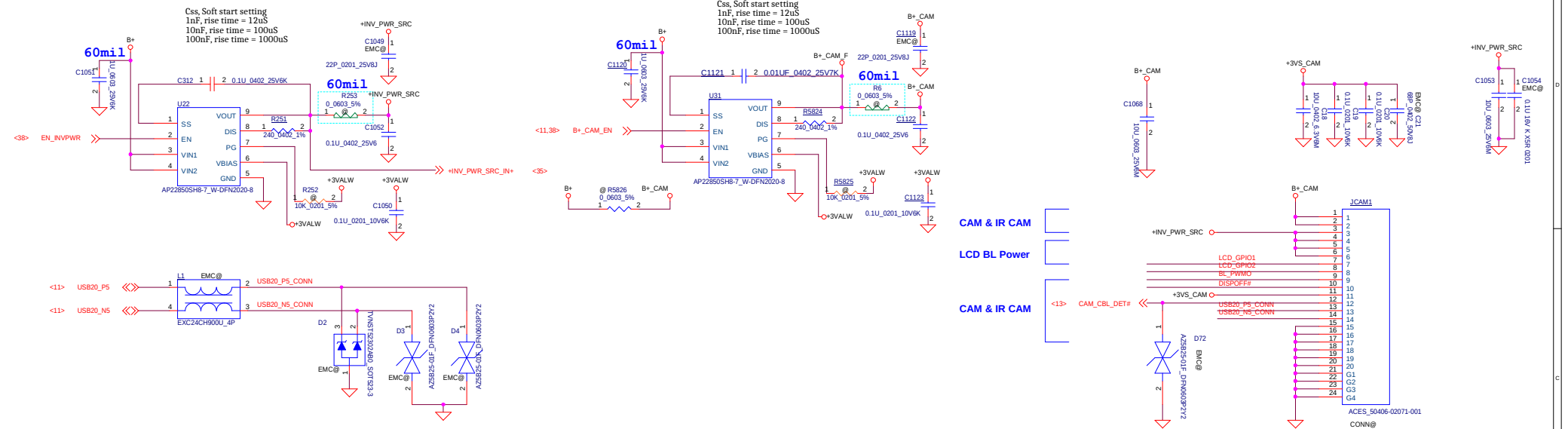


+1.8VA Discharge

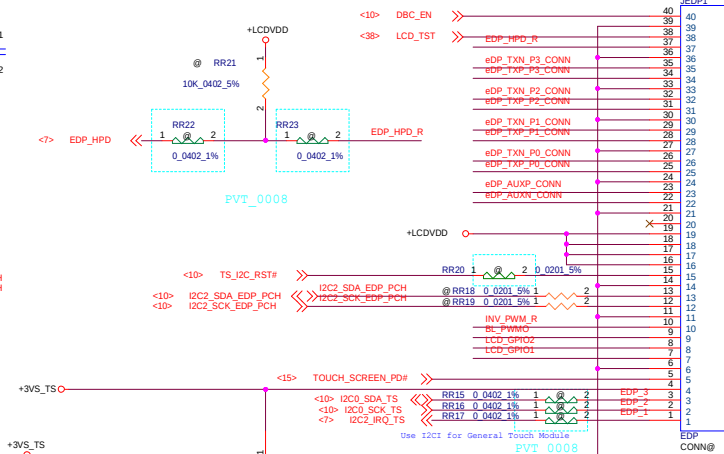
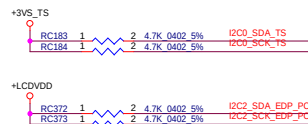
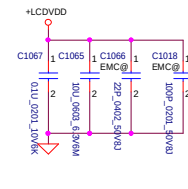


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Title	P36-TP/FP/PWGRGD		
Size	Document Number	Rev	
	LA-E671P	1.0	
Date	Tuesday, October 17, 2017	Sheet	36 of 61

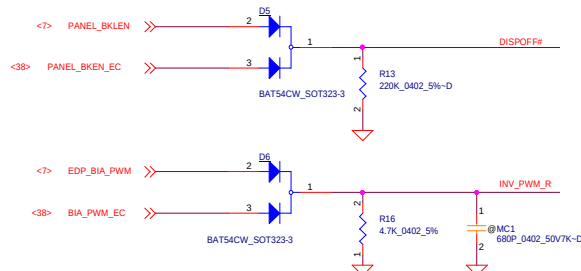
IR Digital CAM / eDP Backlight



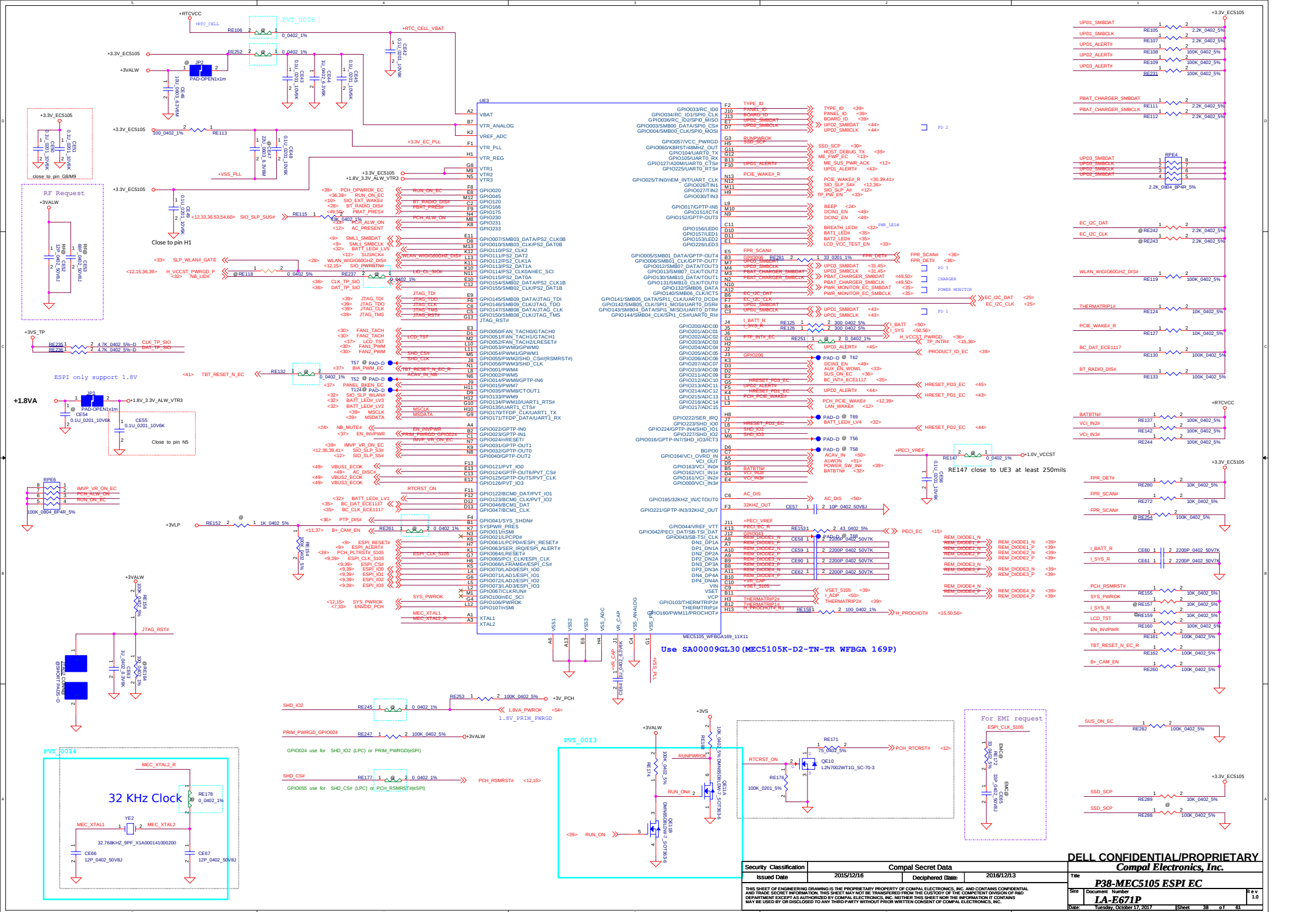
eDP Conn



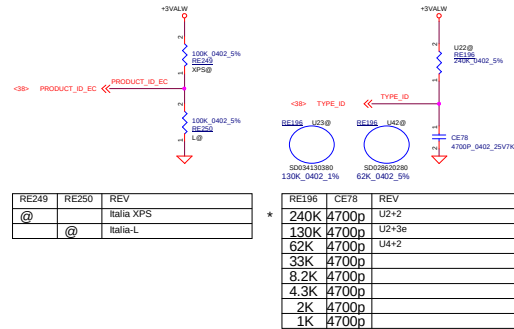
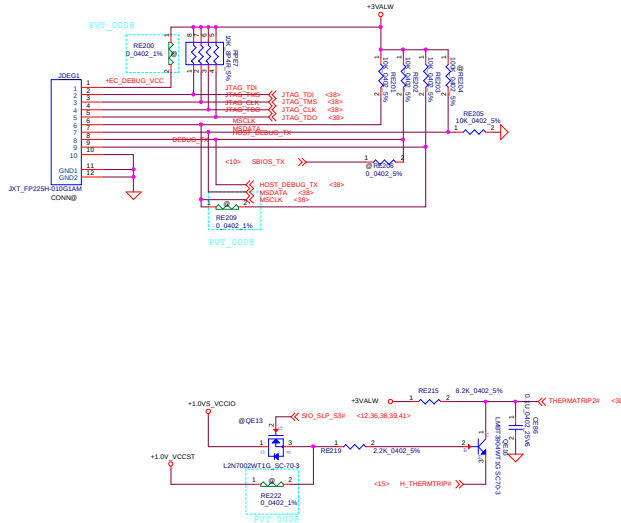
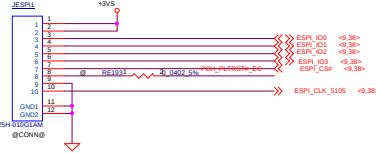
BackLight PWM Control



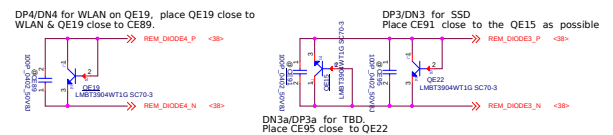
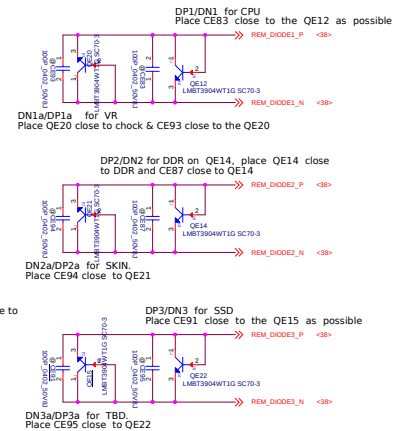
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Issued Date				2041/09/08				Compal Electronics, Inc.			
Deciphered Date				2013/10/28				P37-eDP+TS & CAM+BL CONN			
Title				LA-E671P				Rev 1.0			
Date				Tuesday, October 17, 2017				Sheet 37 of 61			

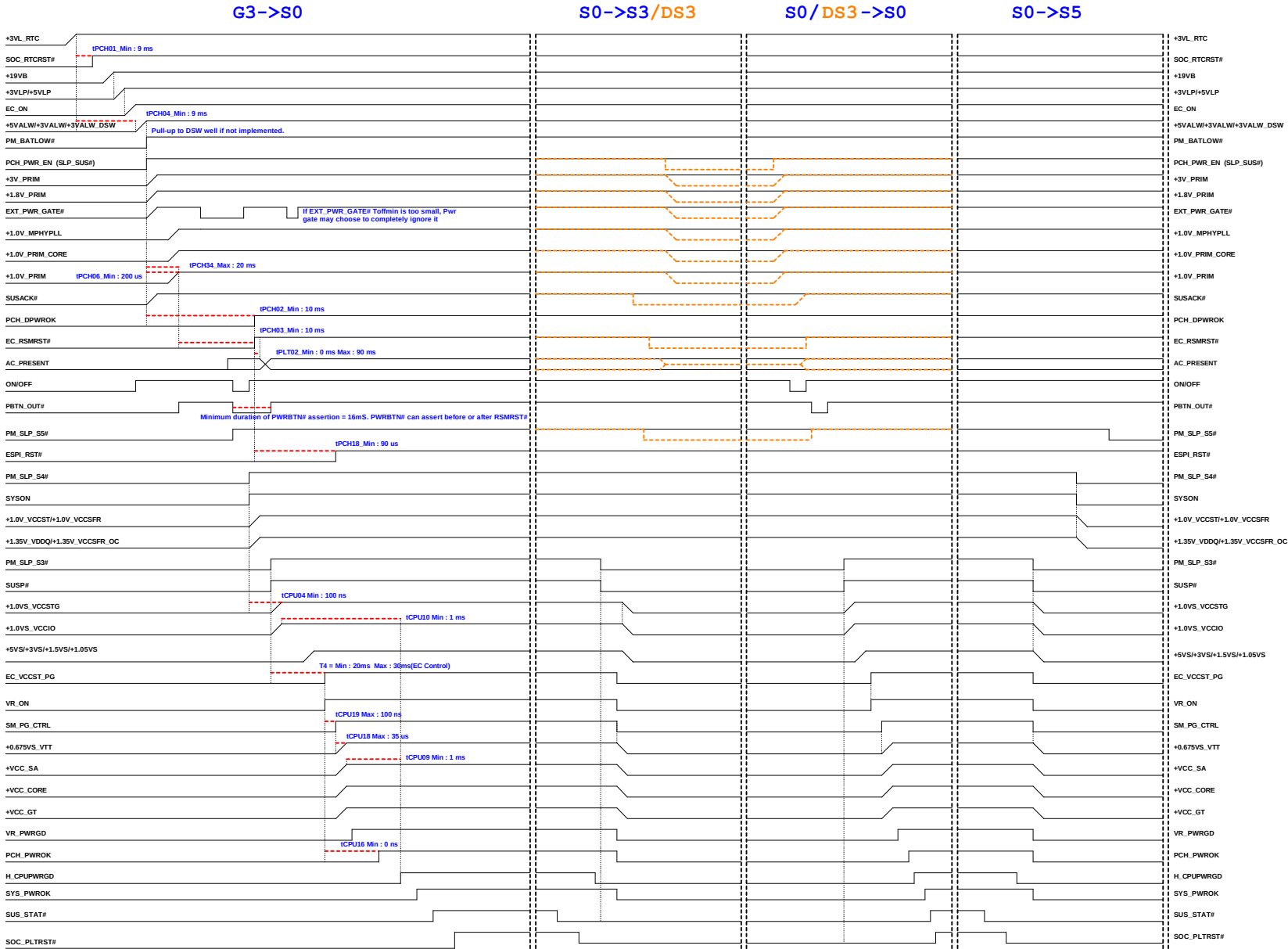


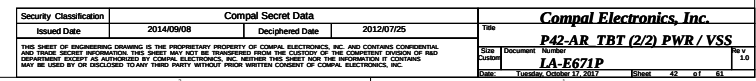
LOC	REFID	VALUE	REFID
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2	U002	U002	U002
3	U003	U003	U003
4	U004	U004	U004
5	U005	U005	U005
6	U006	U006	U006
7	U007	U007	U007
8	U008	U008	U008
9	U009	U009	U009
10	U010	U010	U010

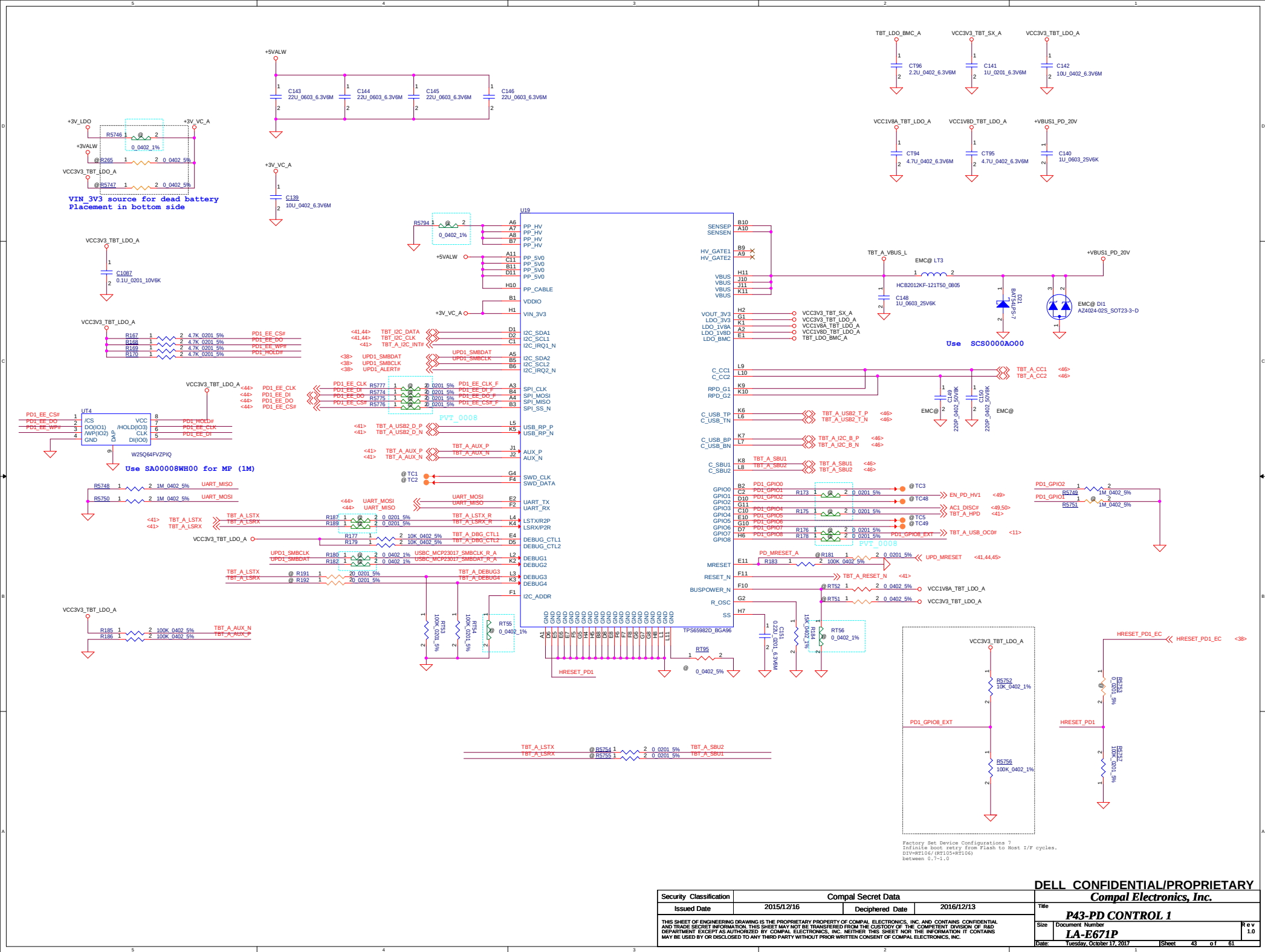


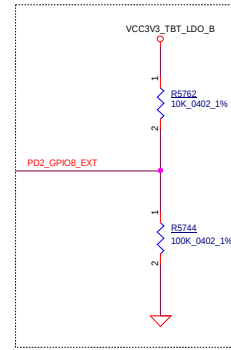
Thermal diode mapping	
5105 Channel Locat bn	
DP1/DN1	OTP (QE12)
SEN4	DN1a/DP1a Charger (QE20)
SEN1	DP2/DN2 DDR (QE14)
SEN5	DN2a/DP2a SKIN (QE21)
SEN6	DP3/DN3 SKIN (QE22)
SEN2	DN3a/DP3a SSD (QE15)
SEN3	DP4/DN4 WLAN (QE19)
	DN4a/DP4a





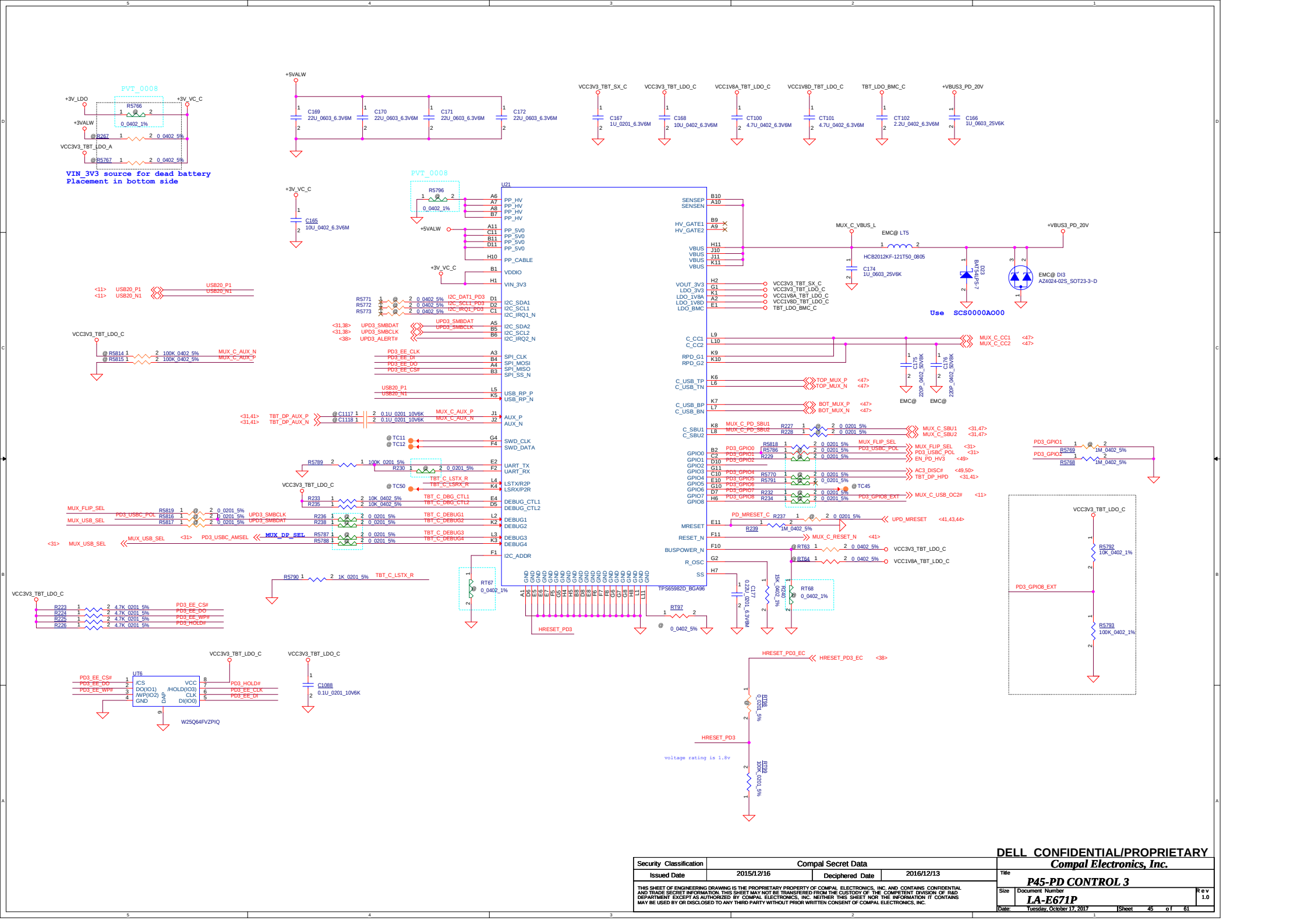


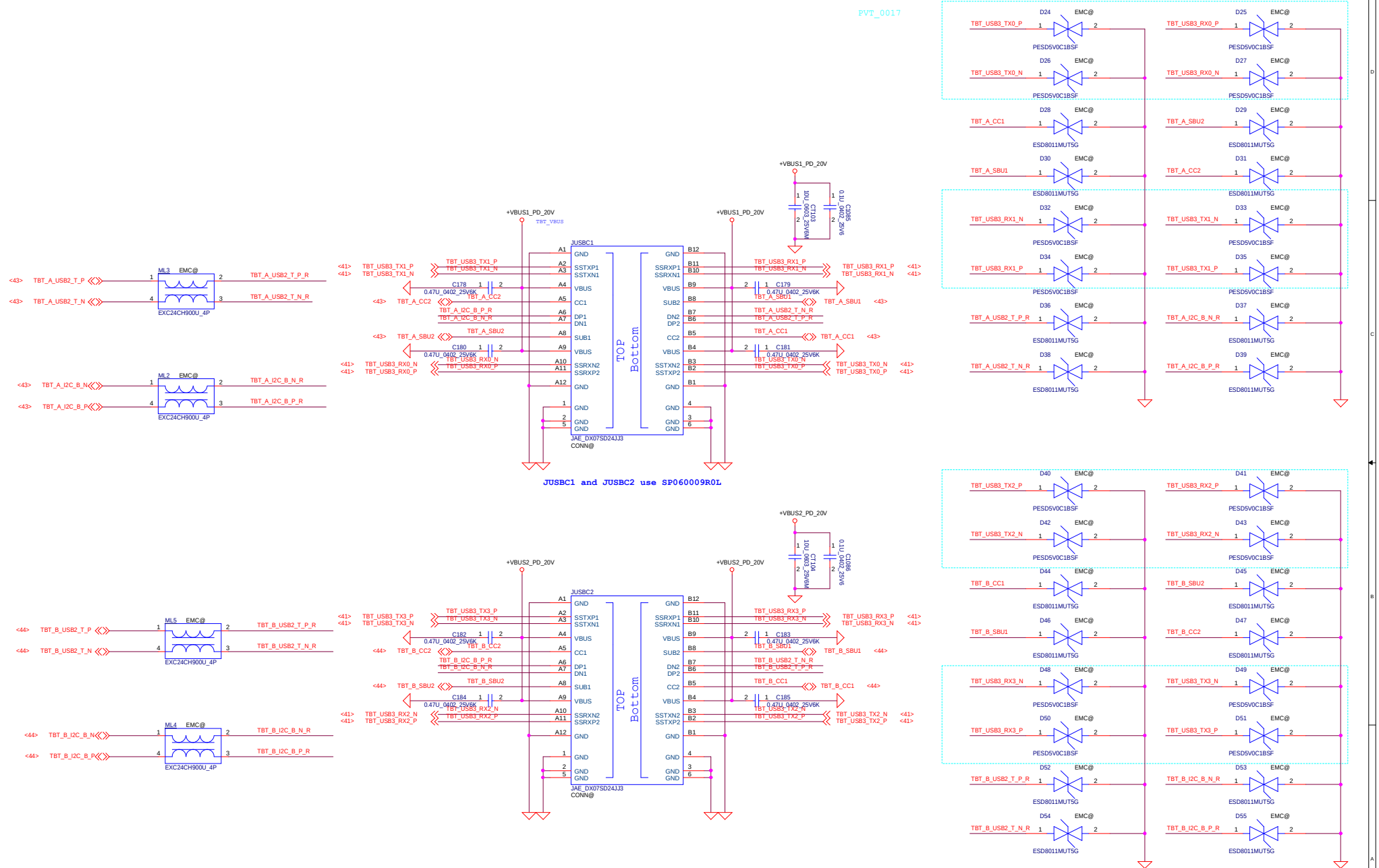


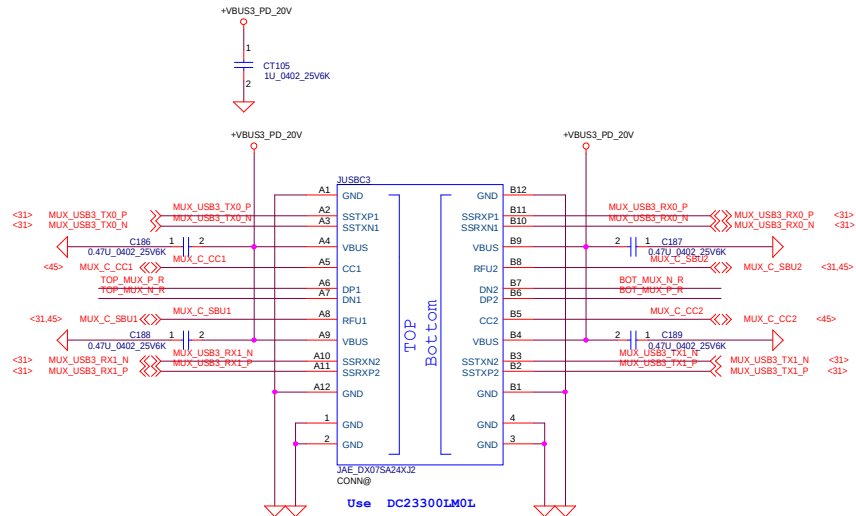
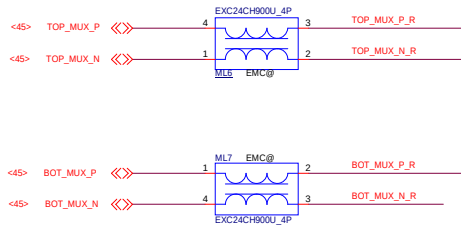


Date:	Tuesday, October 17, 2017	Sheet	44	of	6
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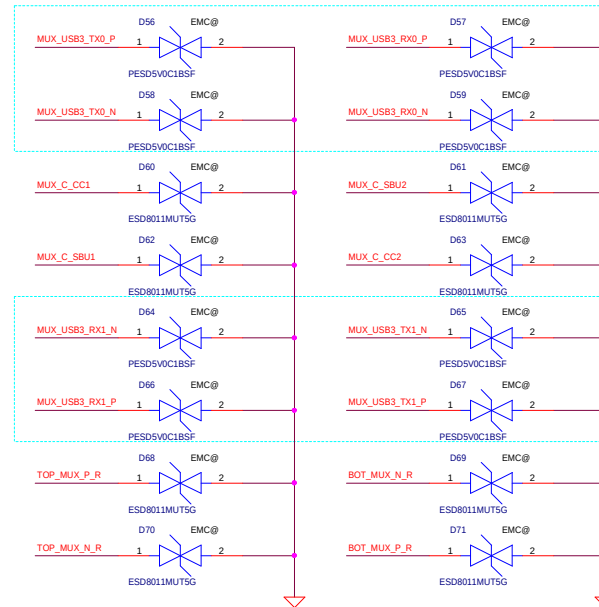
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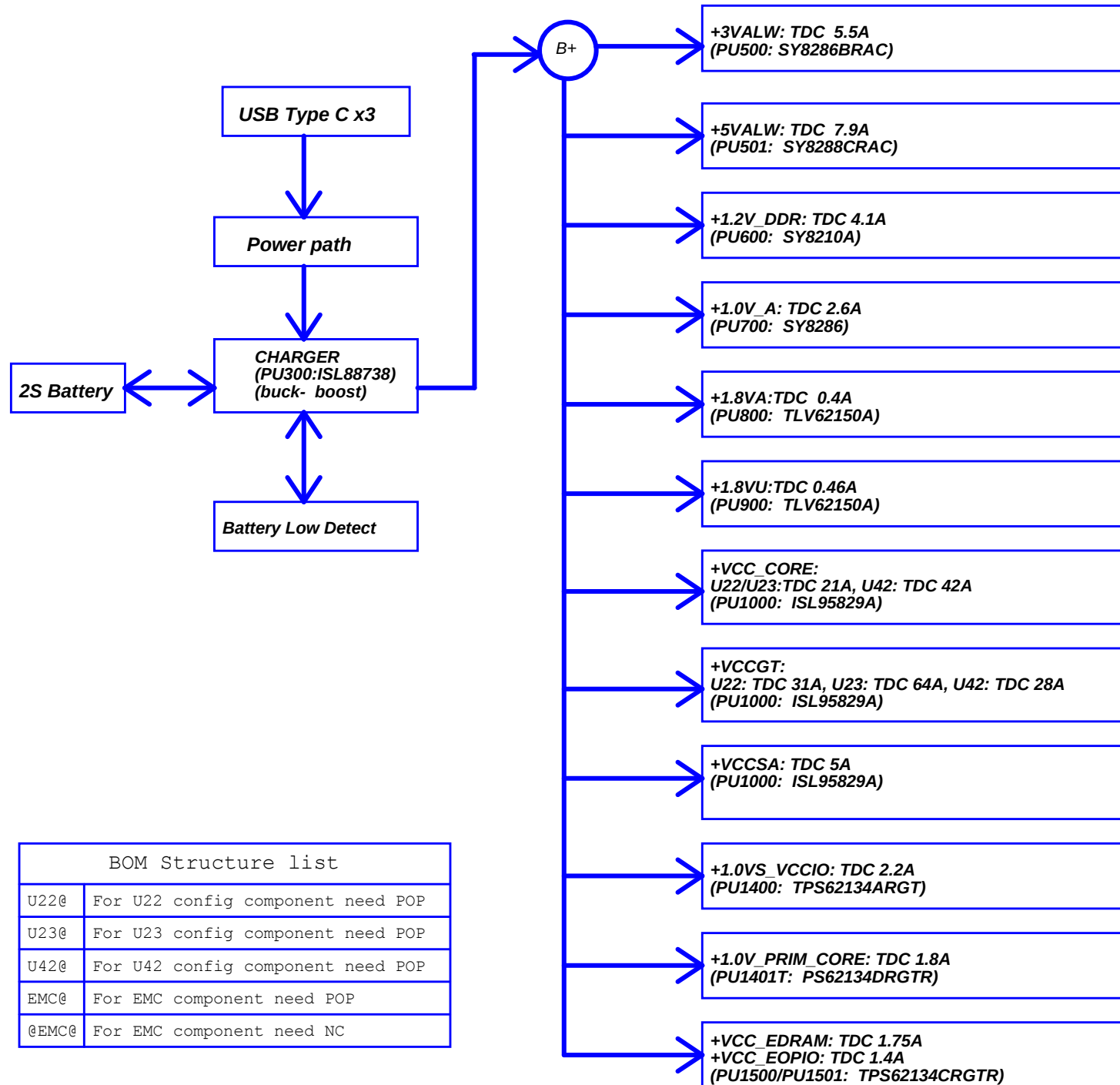


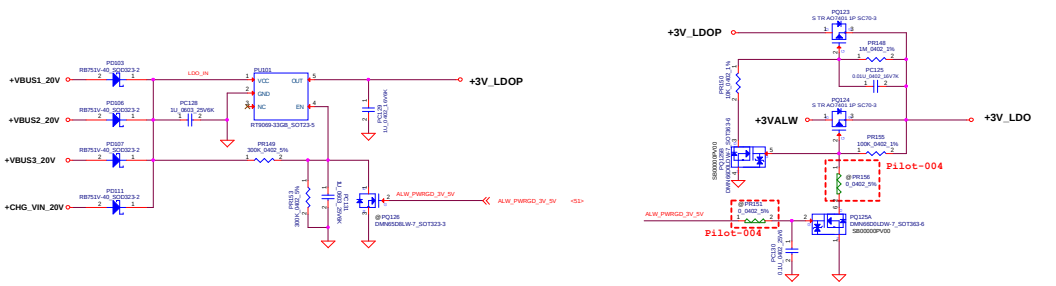
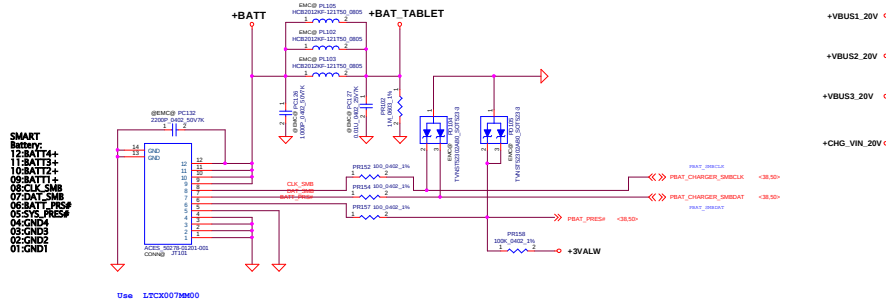
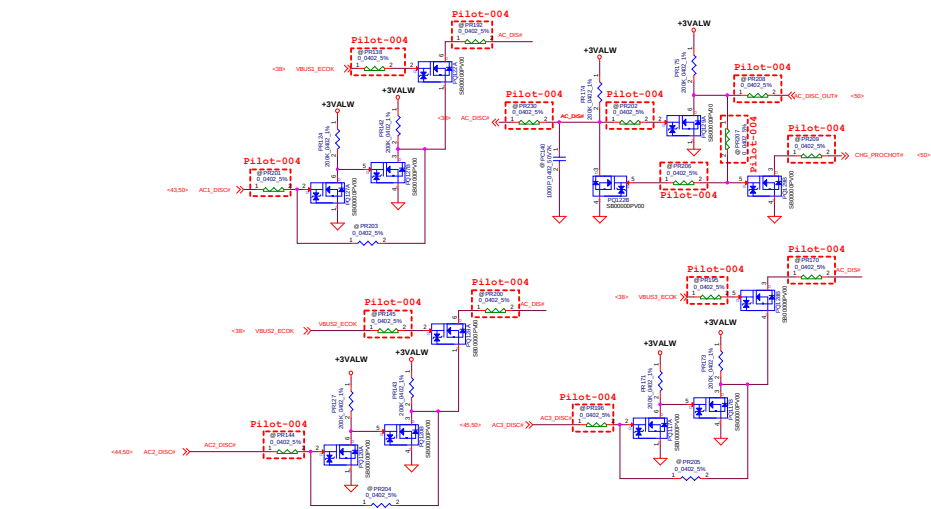
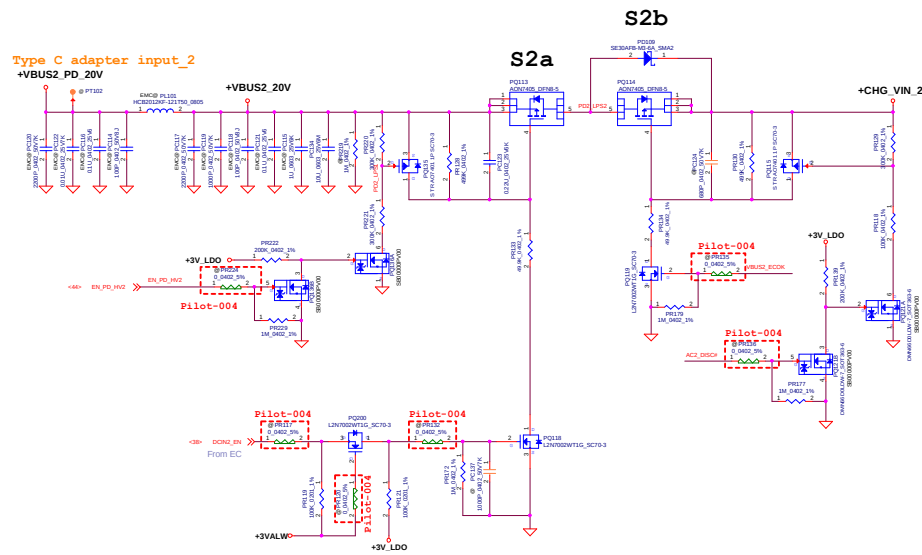
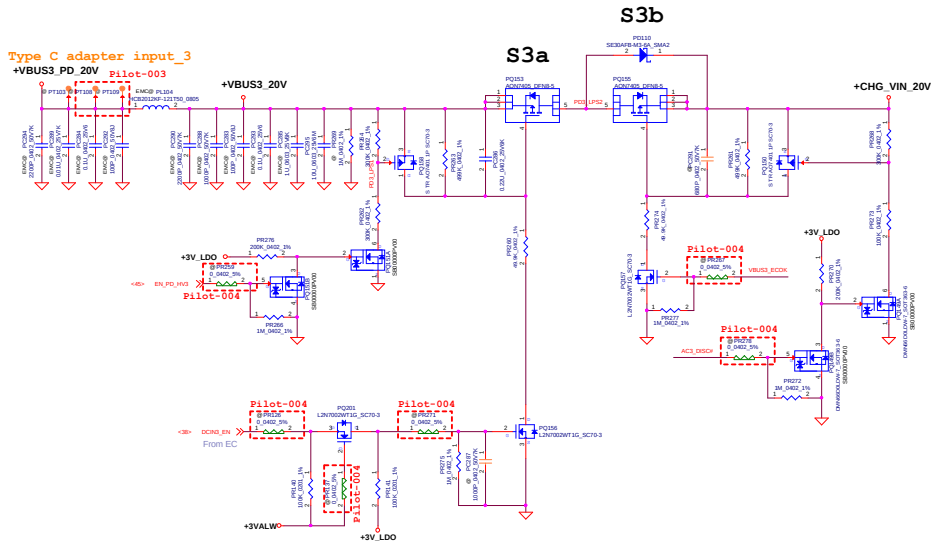
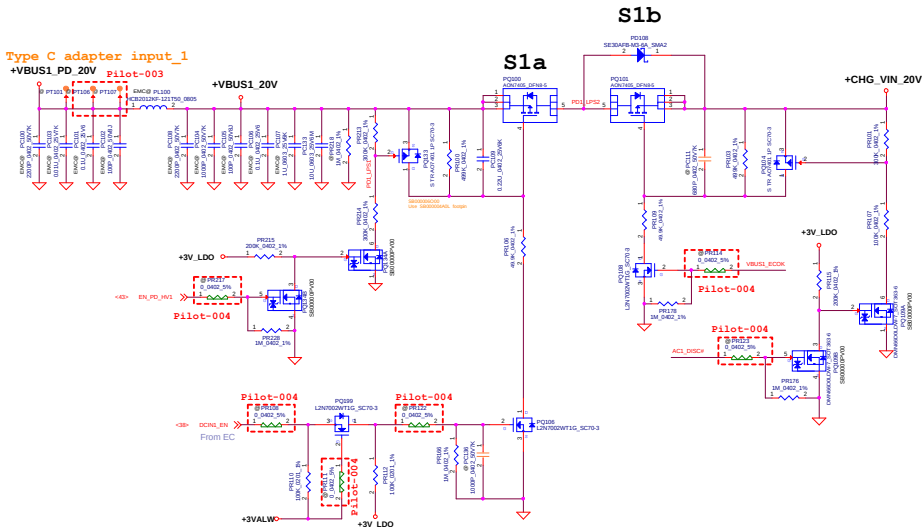




PVT_0017

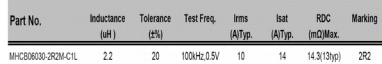




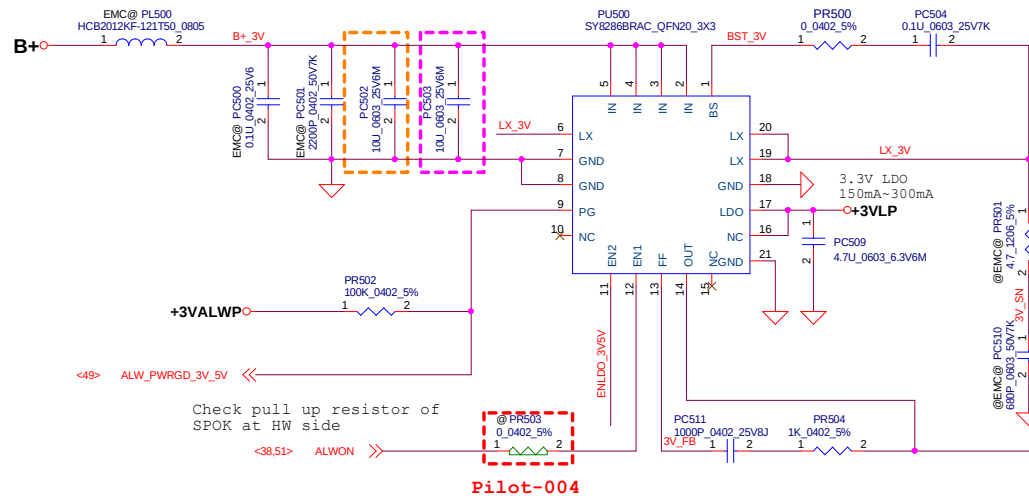


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				Sheet	49 of 61

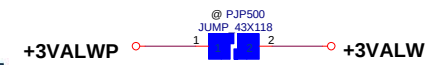
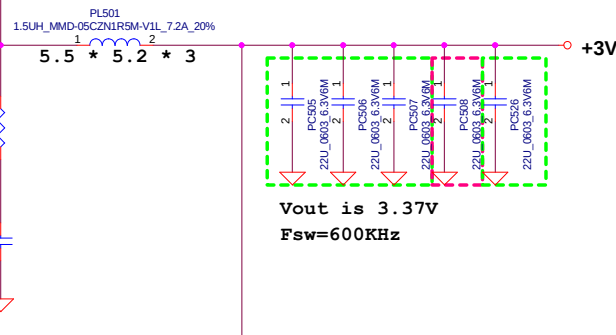
Charger controller(40.1), Support component(40.2)



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	PWR Charger (IS188736)	
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				Document Number	
				LA-E671P	
				Date	Tuesday, October 17, 2017
				Sheet	50 of 61
				Riv	0.2

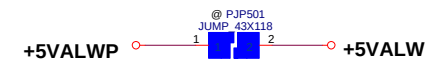


P/N	L*W(mm*mm)	H(mm)	LX(μH)	RDC(mΩ)	I _{ds} (A)	I _{sat} (A)
MMD-05C2-1R5M-V1L	5.49*5.18	3	1.5	19.7	20.7	7.2
			±20%	Typ	Max	Typ

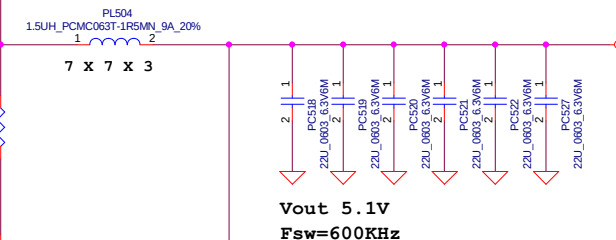
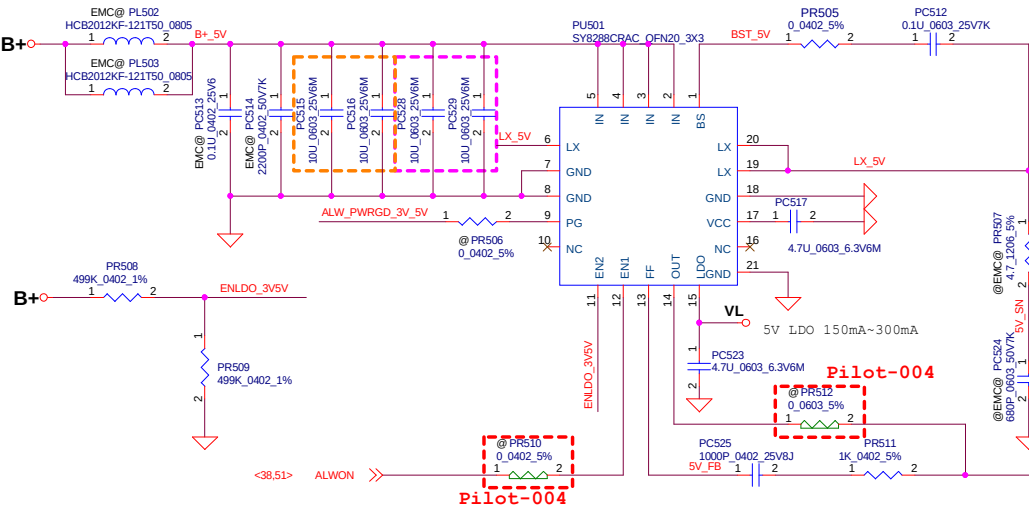


3VALWP
TDC 5.2A
Peak Current 7.5A
OCP Current 8.0A (fix)

Non AR
3VALWP
TDC 5.5A
Peak Current 7.5A
OCP Current 8.0A (fix)

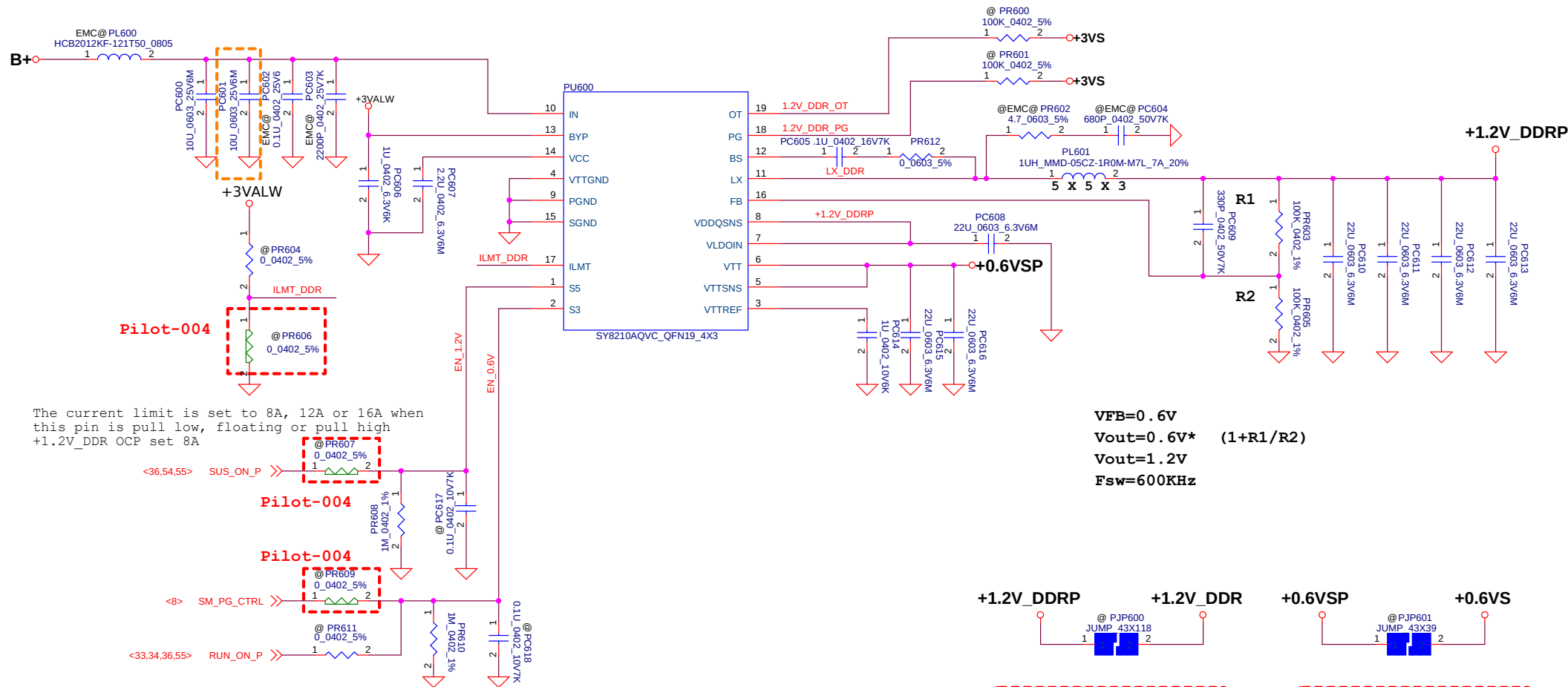


5VALWP
TDC 7.9A
Peak Current 11.0A
OCP Current 13.0A



3V/5V controller(35.1), Support component(35.2)

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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title		
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Size	Document	Number	LA-E671P	Rev	0.4	
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VFB=0.6V
Vout=0.6V* (1+R1/R2)
Vout=1.2V
Fsw=600KHz

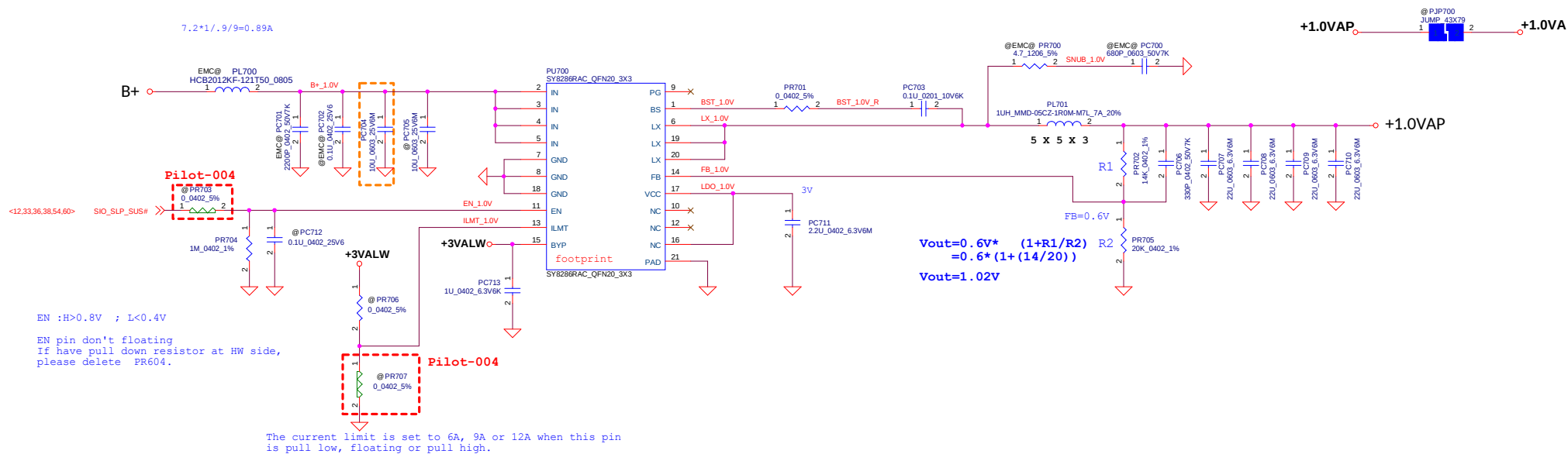
+1.2V_DDR
TDC 4.1A
Peak Current 5.8A
OCP Current 8A

0.6Volt +/- 5%
TDC 0.4A
Peak Current 0.6A
OCP Current 2A (fix)

DDR controller(35.3), Support component(35.4)

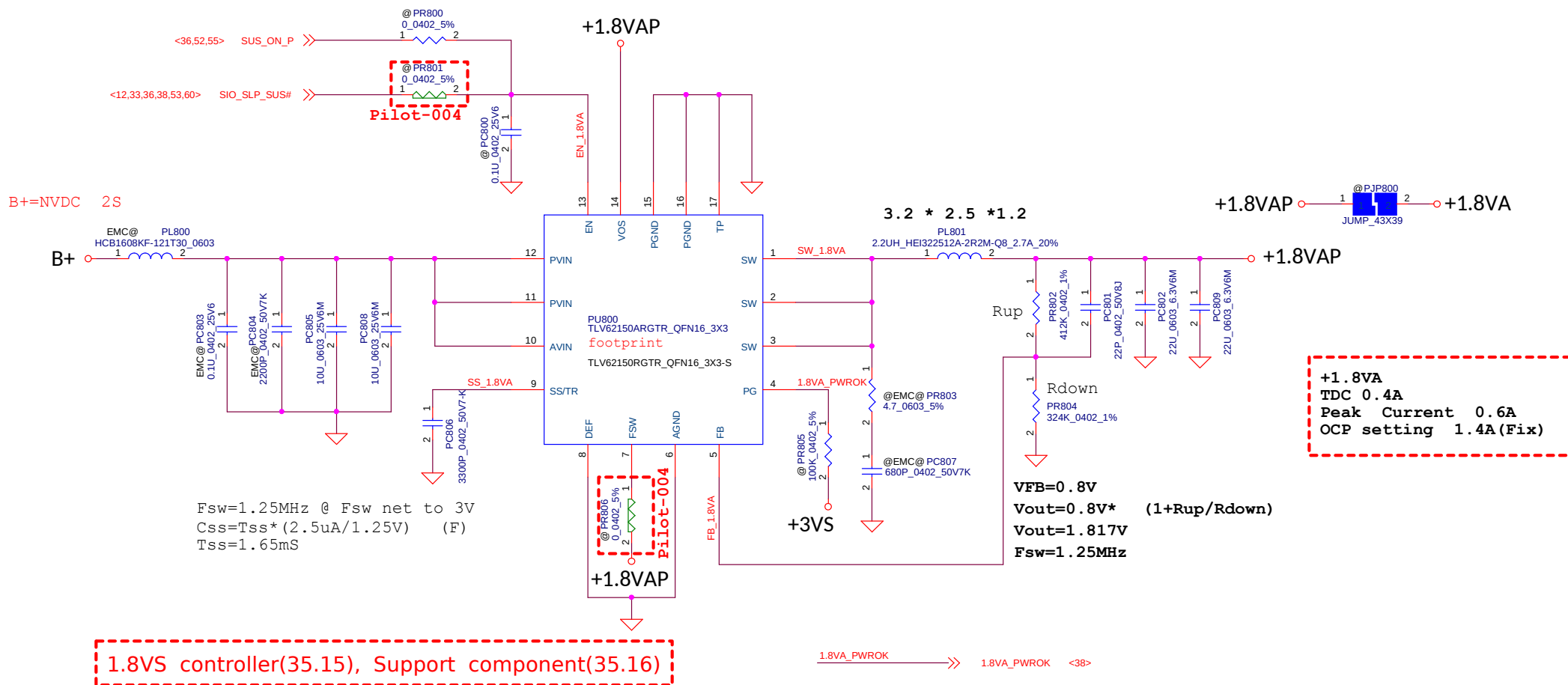
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+1.0VA
TDC 2.6A
Peak Current 3.3A
OCP current 6.0A

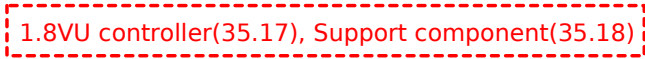


1.05V controller(35.5), Support component(35.6)

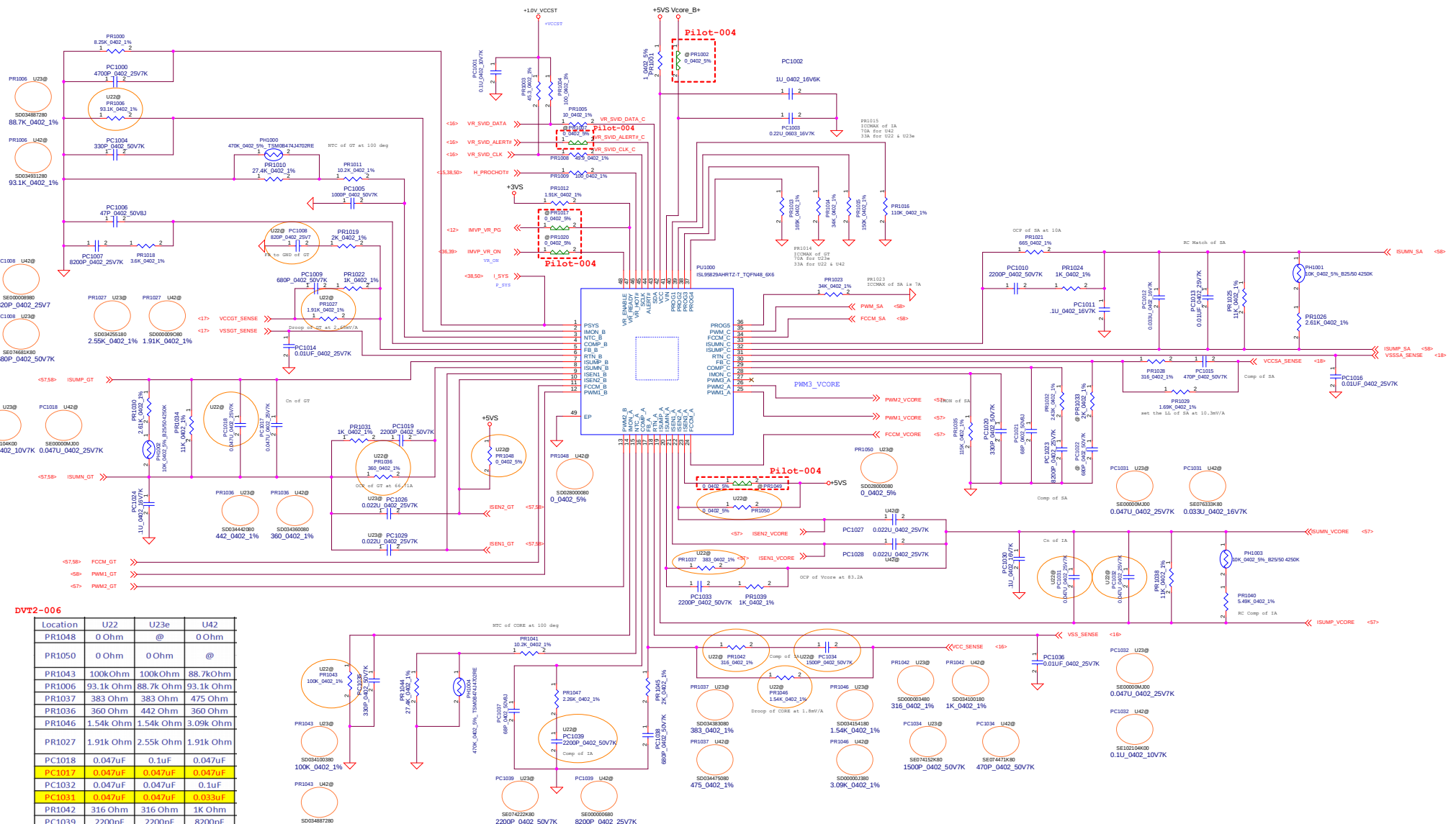
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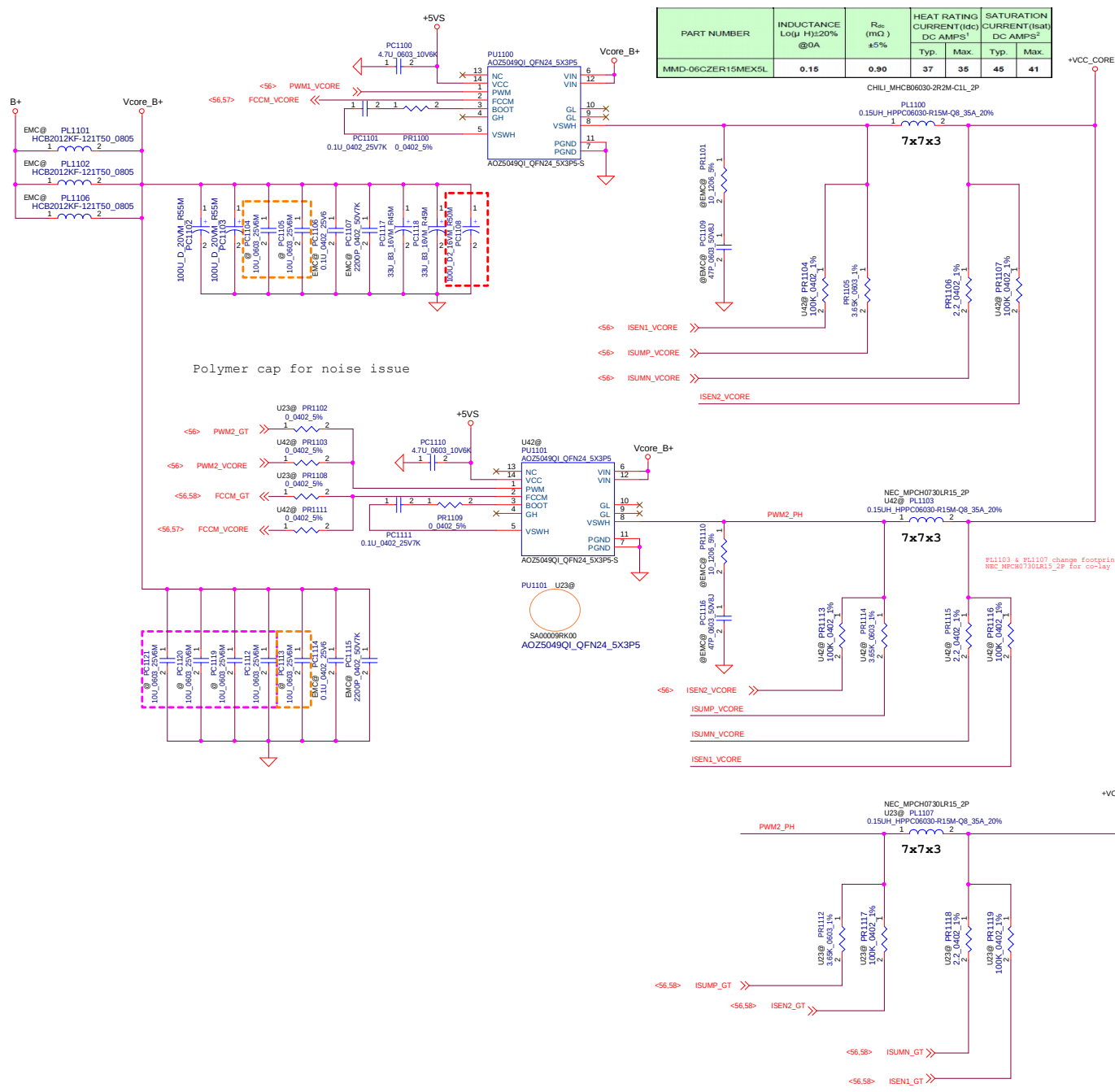
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Location	U22	U23e	U42
PR1048	0 Ohm	@	0 Ohm
PR1050	0 Ohm	0 Ohm	@
PR1043	100k Ohm	100k Ohm	88.7k Ohm
PR1006	93.1k Ohm	88.7k Ohm	93.1k Ohm
PR1037	383 Ohm	383 Ohm	475 Ohm
PR1036	360 Ohm	442 Ohm	360 Ohm
PR1046	1.54k Ohm	1.54k Ohm	3.09k Ohm
PR1027	1.91k Ohm	2.55k Ohm	1.91k Ohm
PC1018	0.047uF	0.1uF	0.047uF
PC1017	0.047uF	0.047uF	0.047uF
PC1032	0.047uF	0.047uF	0.1uF
PC1031	0.047uF	0.047uF	0.033uF
PR1042	316 Ohm	316 Ohm	1k Ohm
PC1039	2200pF	2200pF	8200pF
PR1040	5.49 KOhm	5.49 KOhm	5.49 KOhm
PC1034	1500pF	1500pF	470pF
PC1008	820pF	680pF	820pF

CPU Vcore controller(36.1), Drivers(36.2), Support component(36.3)
Acoustic i Noise B+ Bulk CAP (37.2)

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PART NUMBER	INDUCTANCE Lo(μH)±20% @0A	Rdc (mΩ) ±5%	HEAT RATING CURRENT(I _{dc}) DC AMPS ¹		SATURATION CURRENT(I _{sat}) DC AMPS ²	
			Typ.	Max.	Typ.	Max.
MMD-06CZER15MEXSL	0.15	0.90	37	35	45	41

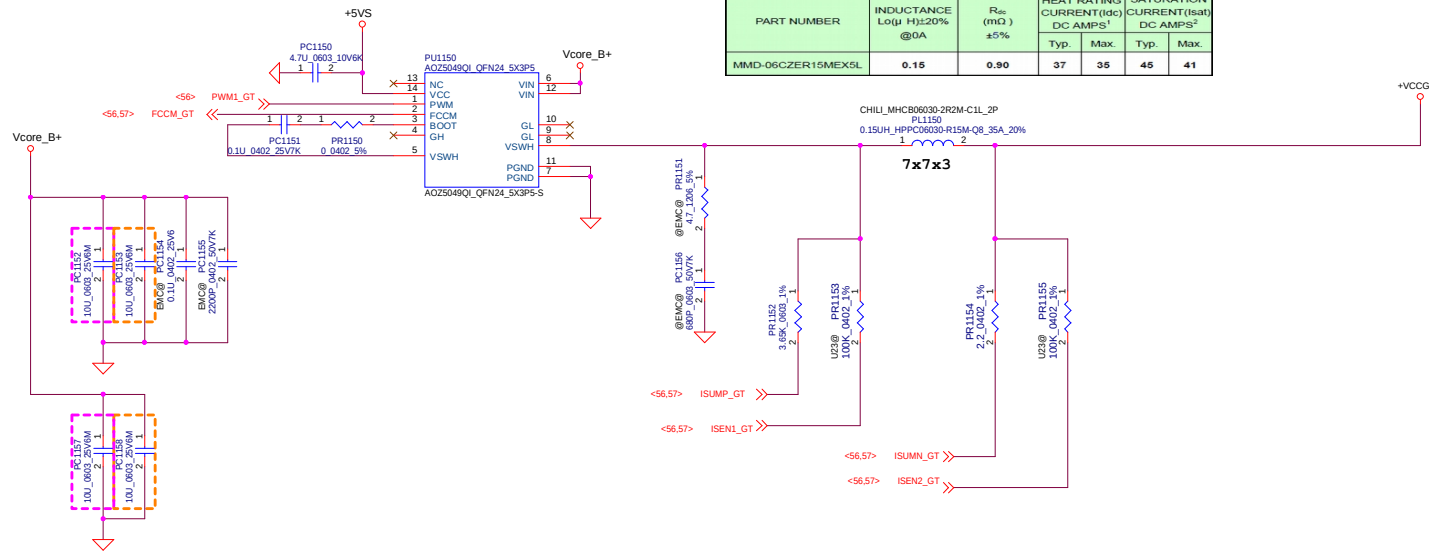
	KBL-RU42 rev.1.6 PAG	KBL-U22 (GT1/GT2) rev.1.5 EDS rev.1.6 PAG	KBL-U23e rev.1.5 EDS rev.1.6 PAG
IA+ring ICCM64	29/32	29	
IA+ring TDC	42	21	
IA+ring di[A]	55	25	
IA+ring DC/A2.4	2.4	2.4	
GT ICCMAX	28	31	64 for merged VR
GT TDC[A]	18	18	38 for merged VR
GT di[A]	20	28	46
GT DC/AC L	3.1	3.1	2
SA ICCMAX	5	4.5	5.1
SA DC/AC L	10.3	10.3	10.3
PL2 extreme	51	29/32	43
PL4 extreme	71	51	66

CPU_Vcore controller(36.1),Drivers(36.2), Support component (36.3), CPU_Core output CAP(36.4),Acoust i cNoise B+ Bulk CAP(37. 2)

VCC_GT (U-line 22)
TDC 18A
Peak Current 31A
OCP current 37A

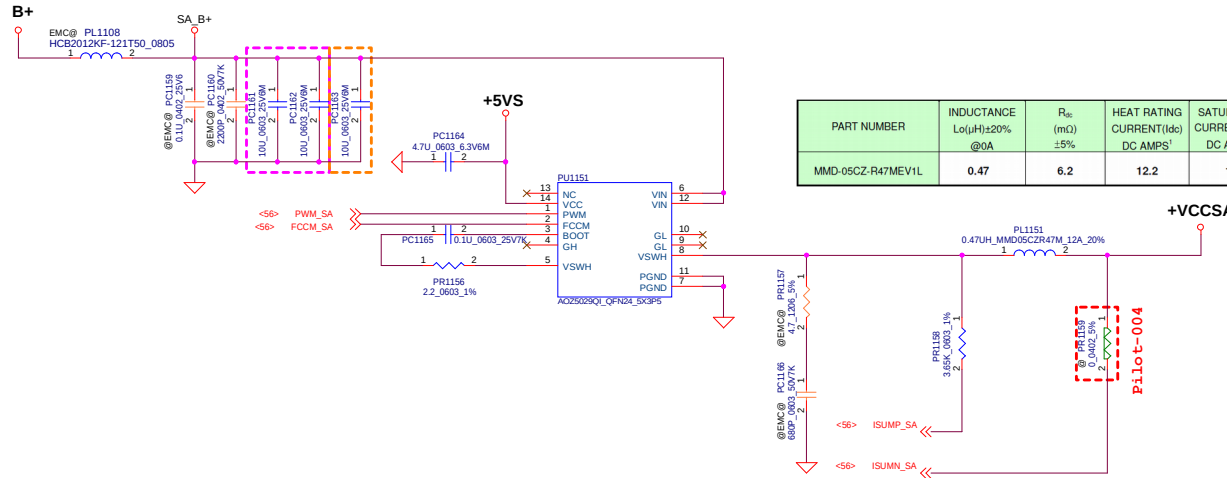
VCC_GT Merged(GT+GTx) (U-line 23e)
TDC 35A
Peak Current 64A
OCP current 74A

PART NUMBER	INDUCTANCE Lo(μ H) \pm 20% @0A	R _{dc} (m Ω) \pm 5%	HEAT RATING CURRENT(I _{dc}) DC AMPS ¹		SATURATION CURRENT(I _{sat}) DC AMPS ²	
			Typ.	Max.	Typ.	Max.
MMD-06CZER15MEX5L	0.15	0.90	37	35	45	41



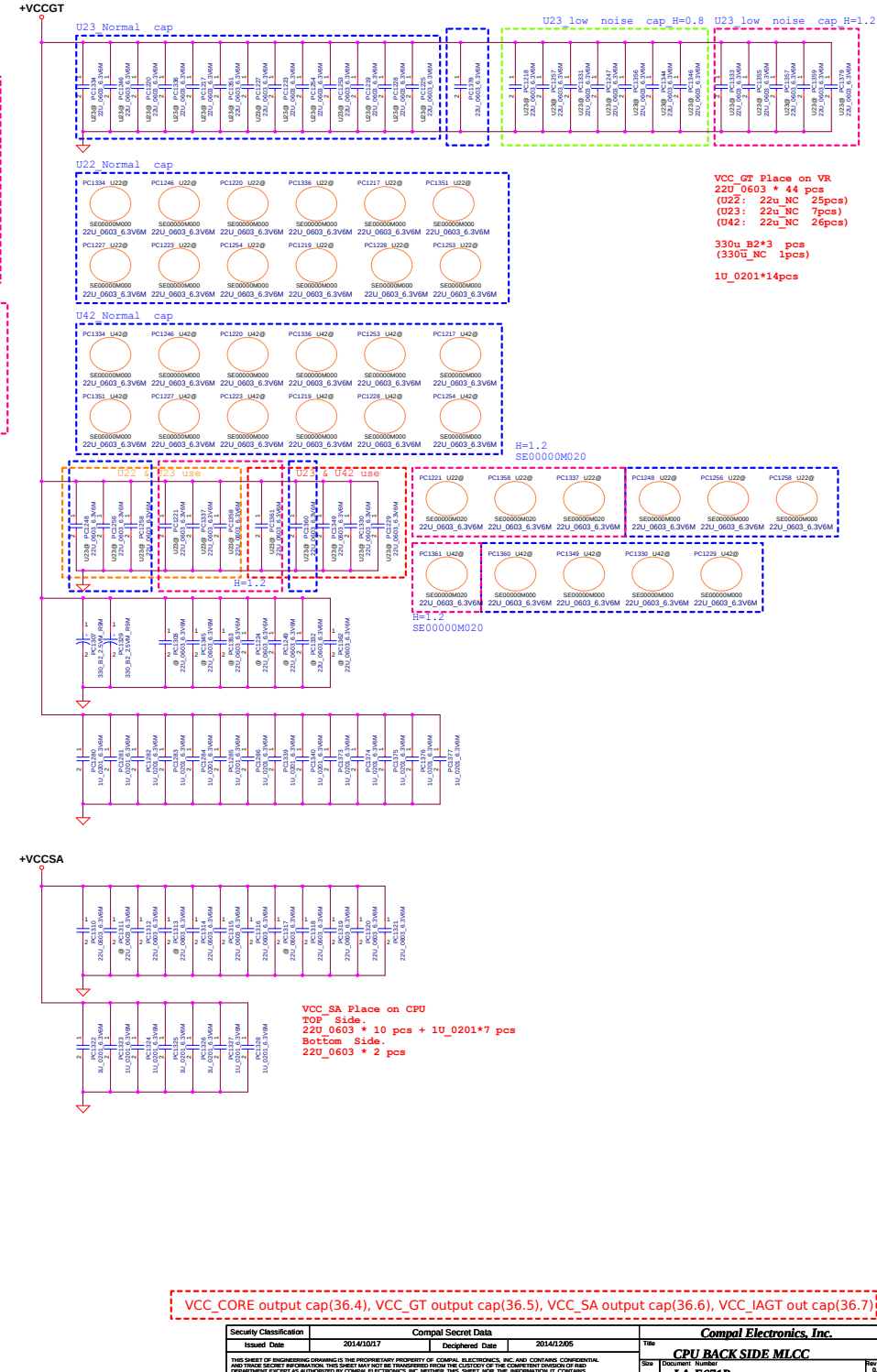
VCC_SA
TDC 5A
Peak Current 5.1A
OCP current 7A

PART NUMBER	INDUCTANCE Lo(μ H) \pm 20% @0A	R _{dc} (m Ω) \pm 5%	HEAT RATING CURRENT(I _{dc}) DC AMPS ¹		SATURATION CURRENT(I _{sat}) DC AMPS ²	
			Typ.	Max.	Typ.	Max.
MMD-05CZ-R47MEV1L	0.47	6.2	12.2		16	



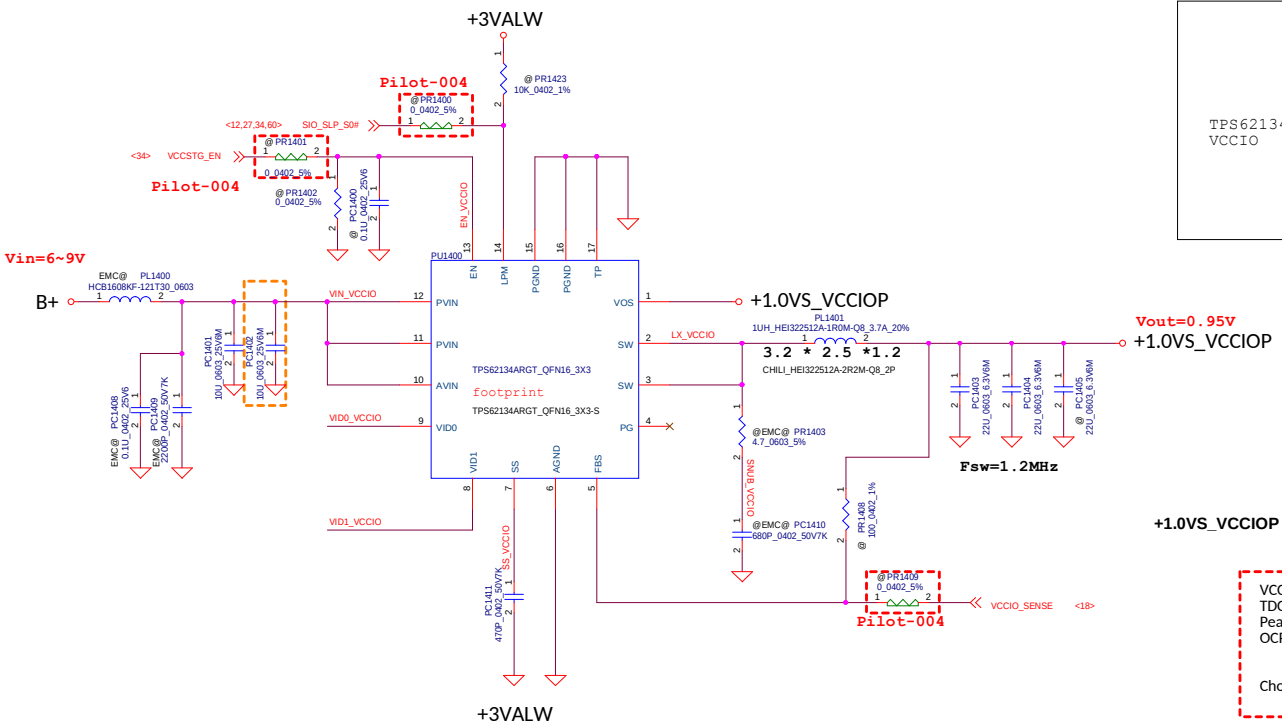
CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
GFX output CAP(36.5)

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	LPM	VID1	VID0	Vout
TPS62134A VCCIO	0	X	X	0.000 (LPM)
	1	0	0	0.850
	1	0	1	0.8750
	1	1	0	0.950
	1	1	1	0.975

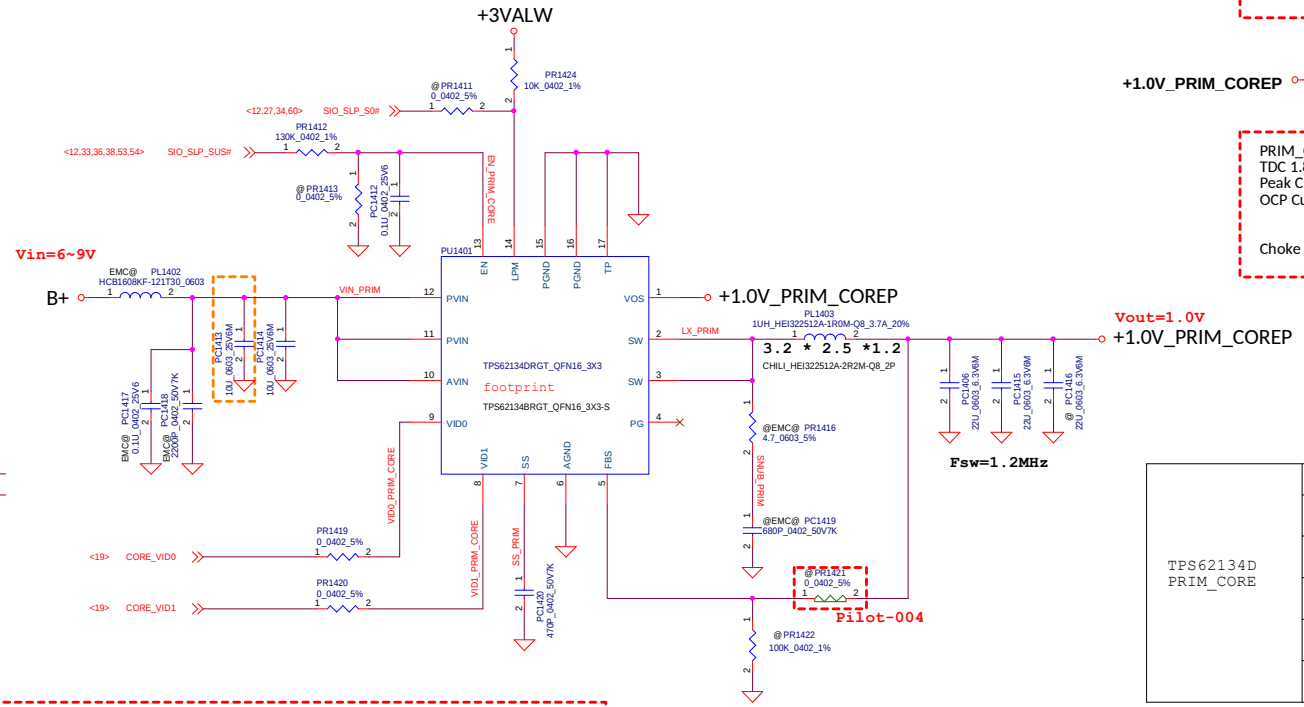


+1.0VS_VCCIO

VCCIO
TDC 2.2A
Peak Current 3.1 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 34.0mohm

+1.0V_PRIM_CORE

PRIM_CORE
TDC 1.8A
Peak Current 2.6 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 34.0mohm



+1.0V_PRIM_CORE

	LPM	VID1	VID0	Vout
TPS62134D PRIM_CORE	0	X	X	0.700 (LPM)
	1	0	0	0.850
	1	0	1	0.900
	1	1	0	0.950
	1	1	1	1.000

+1.0VS VCCIO controller(35.21), Support component(35.22)
+1.0V_PRIM_CORE controller(35.23), Support component(35.24)

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